ECE 126 – Inverter Tutorial: Identifying Static and Dynamic Power in a CMOS Inverter
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Objectives

- **Measure Static Power Dissipation in a CMOS Inverter using Cadence**
- **Measure Total Power Dissipation in a CMOS Inverter using Cadence**
- **Calculate Static Power Dissipation in a CMOS Inverter using Cadence**

Background

The total power dissipation of a circuit includes both a dynamic and a static component that can be challenging to isolate from each other in simulations. Consider the CMOS inverter shown below. The dynamic power is due to switching currents required to charge/discharge output loads and short circuit (direct path) currents that flow between the pMOS and nMOS transistors as the input signal changes. The static power is due to leakage sources in the transistors, including subthreshold conduction between source and drain and reverse bias pn-junction leakage between the source/drain and substrate, which are illustrated in the transistor figure below.

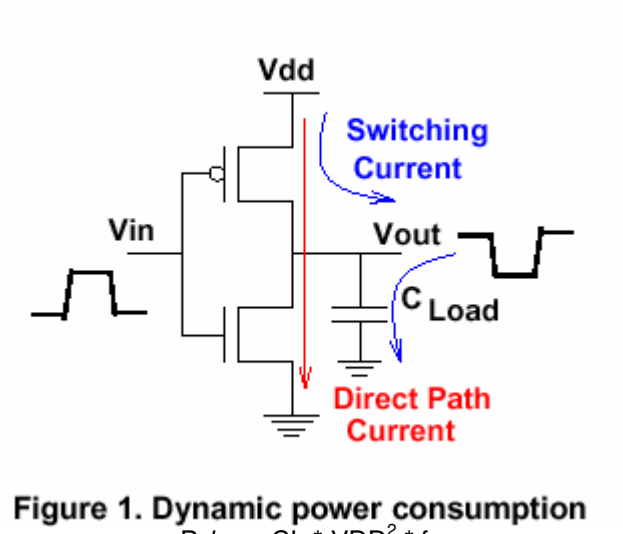


Figure 1. Dynamic power consumption

$P_{dyn} = CL * VDD^2 * freq$

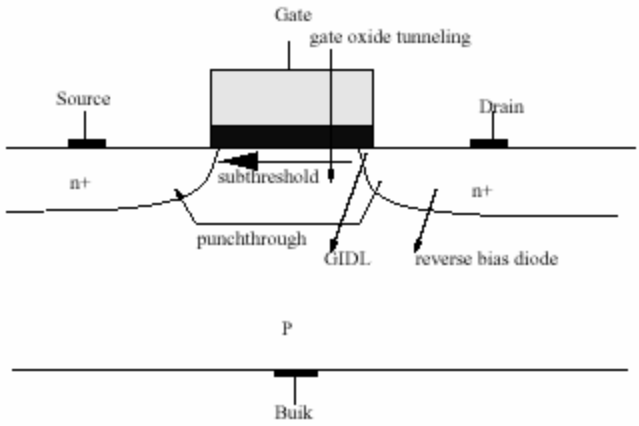


Figure 2. Static CMOS Leakage sources

$P_{stat} = I_{stat} * VDD$

To measure the static power dissipation, we simply apply a static (DC) input signal so that no switching occurs. For digital circuits, this amounts to a high (VDD) or low (ground) at the input, which typically turns one side of the circuit off and eliminates any static short circuit current through the transistors. For analog circuits, the input should be set to the appropriate DC operating point of the circuit, typically somewhere between ground and VDD. This is one of the reasons that analog circuits consume more power; in their static state many transistors are turned on and consume static power.

Example: For a CMOS inverter with pMOS 1.5u/0.6u and nMOS 1.5u/0.6u and a 5pF load capacitance (fig X.X below), we can use the *Simple Method* described below to measure the static power dissipation by applying a high (3.3V) or low (0V) input signal.

if Vin = 3.3V Pstat = 10.94E-12 W,
if Vin = 0V Pstat = 10.93E-12 W.

Notice that, as you should expect, the power consumption is nearly the same for both cases. The difference is due the slightly different leakage in pMOS and nMOS transistors when they are biased with different voltages. We could expect these results to vary more if one of the transistors were much larger than the other.

To measure **total** power dissipation, we have to apply an input signal that varies with time, causing the output node to charge/discharge. For digital circuits this simply requires applying a pulse input signal.

Example: For a CMOS inverter with pMOS 1.5u/0.6u and nMOS 1.5u/0.6u and a 5pF load capacitance, we can use the *Simple Method* described below to measure the static power dissipation by applying a pulse input that changes from VDD to ground.

if Vin is a pulse (pulse width = 5µs, period = 10µs).. P*total* = 5.49uW.

Notice that if we remove the load capacitor the switching current is reduced to only that needed to charge/discharge the parasitics at the output, and as a result the measured power will be much closer to the value measured for static power.

For analog circuits, this approach is complicated by the fact that the inputs to analog circuits do not typically switch from high to low like digital circuits. To use this method on analog circuits, one must first determine the typical input signal swing and then apply the appropriate input signal, which in many cases would be an AC signal (often with a DC bias). The *Alternative Method* described below may be more useful for measuring the total power dissipation in analog circuits. However, it is important to note that power dissipation in most analog circuits is dominated by the static power, so applying the appropriate DC bias to all inputs and measuring static power may be sufficient in many cases.

To measure dynamic power dissipation, we can subtract the static power from the total power to estimate the contribution of dynamic sources.

Measuring Static Power Consumption Using Cadence:
Simple Method

- Create the following test bench for the inverter you created in lab 1 (DC = 3.3V),
    - set VDC=0 – this will test the PMOS device first

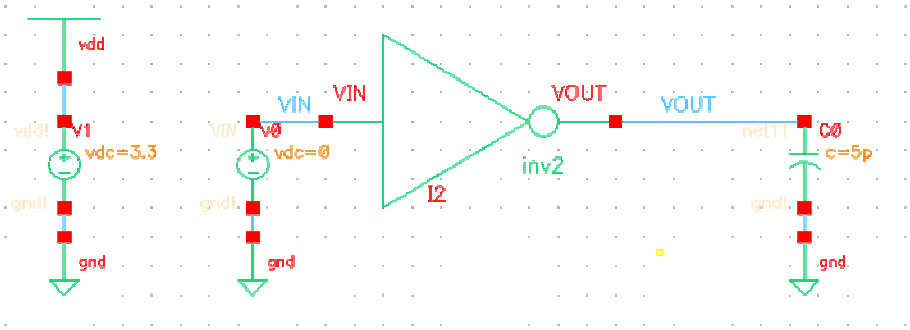
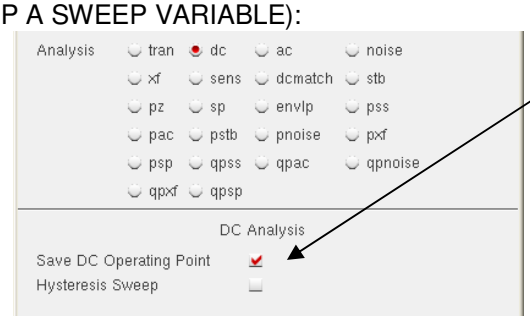
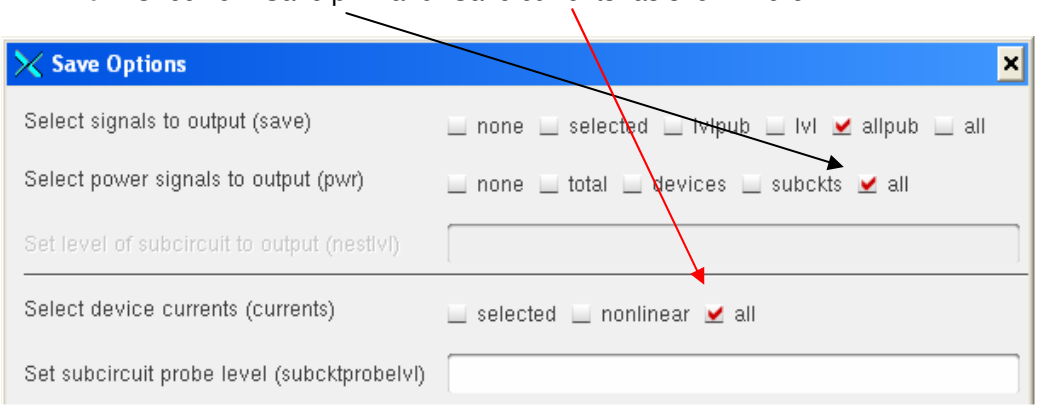


Figure 1.1 – Test Bench

- Using the SPECTRE simulator, set up a DC analysis ensure you check: *Save DC Operating Point* (DO NOT SETUP A SWEEP VARIABLE):



- From the simulator menu, choose: Ouptuts->Save All…
    - Check off “Save pwr” and “Save currents” as shown here:



- Run the simulation, ensure there are no errors in the CIW window
    - There will not be anything plotted during the simulation
- When the simulation is complete:
    - From the simulator menu, choose: Results->Annotate->DC Node Voltages
    - From the simulator menu, choose Results->Annotate->DC Operating Points
    - Both the node voltages and currents will be annotated on the schematic
- Return to the schematic window and look at the VDD terminal:
    - The voltage across the inverter is 3.3 V, and the current drawn by the inverter is 3.313pA.
    - Using the formula, P*stat* = I*stat* * VDD, we have 10.9pWatts of power drawn by the PMOS device (see figure 1.2
    - Repeat the simulation with VIN = 3.3V, this will turn the NMOS device on and the PMOS device off

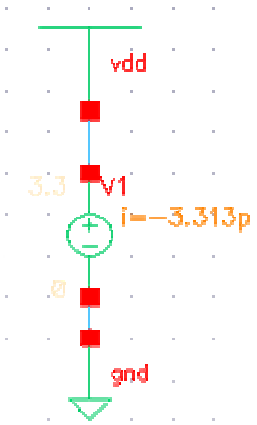


Figure 1.2 – Static Power Diispation of PMOS device in Inverter

Alternative Method

- Alternatively you can find the static power directly by choosing (from the simulator menu): Tools->Results Browser
- A window BROWSE PROJECT HIERARCHY will pop up. Click OK.
- Click on dcOpInfo-Info->V1->pwr, you will see the power agrees with your calculation: 10.9pW, note: V1 is the vsource attached to VDD (make sure this is the same in your schematic!)

Measuring Total Power Consumption Using Cadence:

- Create the following test bench for the inverter you created in lab 1 (DC = 3.3V),
    - Set VDD = 3.3V
    - Set VPULSE = 0 to 3.3V, pulse width=5us, period = 10us

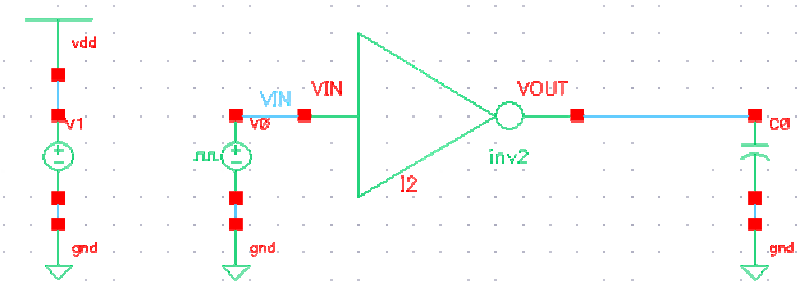
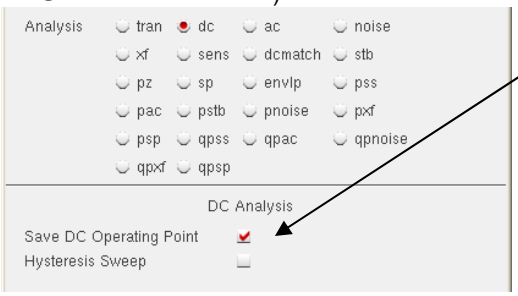
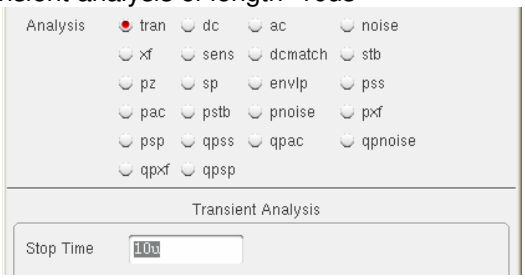


Figure 1.3 – Total Power Dissipation Test Bench

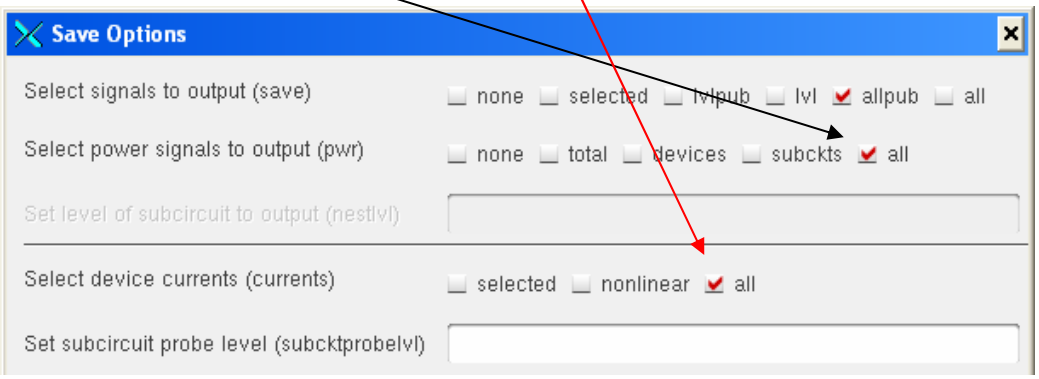
- Using the SPECTRE simulator, set up a DC analysis ensure you check: *Save DC Operating Point* (DO NOT SETUP A SWEEP VARIABLE):



- In addition, setup a transient analysis of length=10us

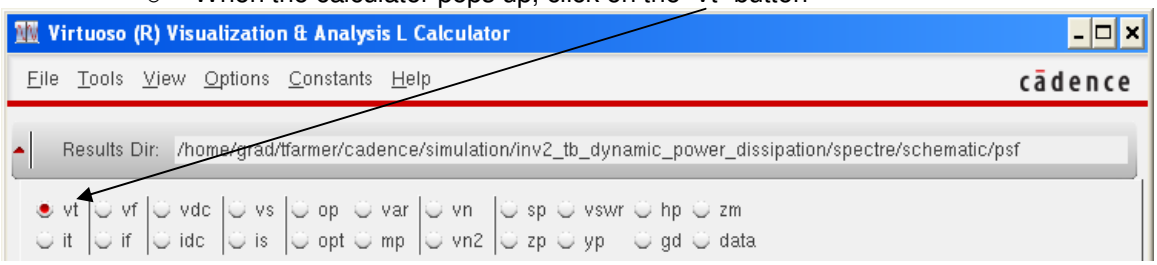


- From the simulator menu, choose: Ouptuts->Save All…
    - Check off “Save pwr” and “Save currents” as shown here:

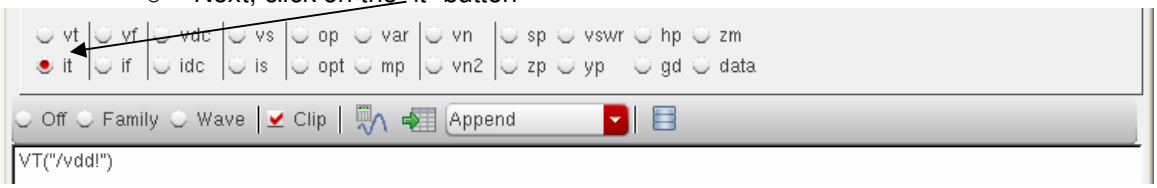


- Run the simulation, ensure there are no errors in the CIW window
    - There will not be anything plotted during the simulation

- When the simulation is complete, from the simulator menu choose: Tools->Calculator
    - When the calculator pops up, click on the “vt” button

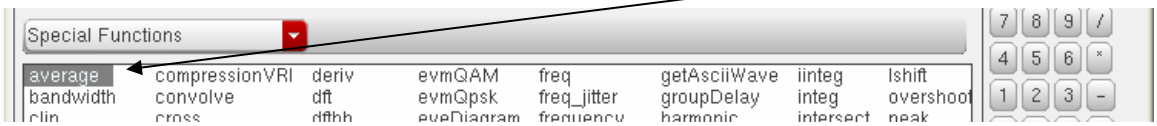


    - You will be returned to the schematic, click on the blue wire connecting VDD to its VDC source
    - The calculator will be populated with: VT(“/vdd!”)
        - Meaning ‘transient voltage of net vdd!
    - Next, click on the “it” button

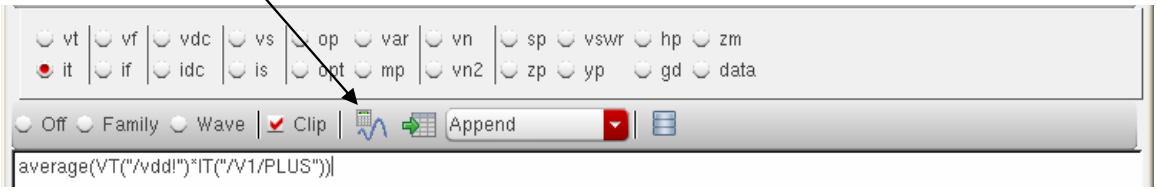


    - You will be returned to the schematic, click on the top red terminal connecting of the VDC connected to VDD
    - The calculator will be populated with: IT(“/V1/PLUS”)
        - Meaning ‘transient current of the instance V1 (note your source may have a difference instance name, like V2, V3, etc)
    - From the calculator pad, click on the * symbol to multiply these two signals together

    - Under the “Special Functions” category, click on the “average” function



    - You have now built the expression shown in the calculator below. Press the ***evaluate*** button to evaluate the expression.



- The total power should be calculated to be about: 5.49uWatts

Measuring Dynamic Power Consumption Using Cadence:

- We found the total power consumed by the inverter (when loaded with a 5pF cap) to be about 5.49uWatts.
- To determine the dynamic power we simply subtract the static power from the total power: 5.49uW-10.94E-12 W ≈ 5.48uWatts
- There isn't much of a difference because most of the power consumed in CMOS technology is done during the switching cycle (dynamic power).
- If we hand calculated the dynamic power dissipation for this device using the formula for dynamic power: $P_{dyn} = CL * VDD^2 * freq = 5pF * 3.3^2 * (1/10us) = 5.45uW$, we see the formula isn't too far off from our simulation!