ECE 126 – Inverter Tutorial: Layout, DRC, Extraction, and LVS

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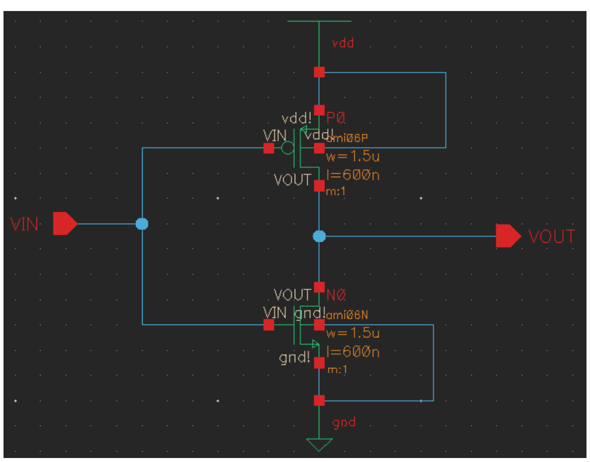
Document Contents

Introduction

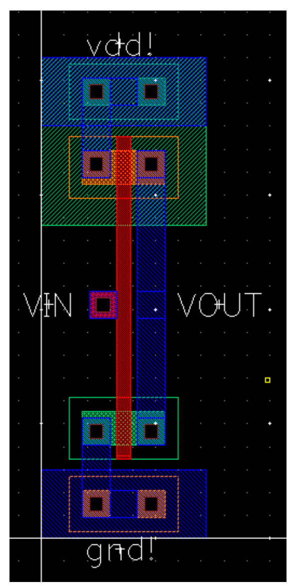
This tutorial demonstrates how to complete the physical design (layout), design rule check (DRC), parameter extraction, and layout vs. schematic (LVS) using the Cadence tools. These operations are performed step-by-step to complete the design of an inverter cell, began in Tutorial A, using the design rules for the AMI C5N (□=0.3) fabrication process. Techniques and tips for using Cadence layout tools are presented.

It is important that you always have a verified functional schematic before beginning layout. If the schematic is not correct, the layout will also be incorrect. As shown in the figure below, the layout should contain the same pin names and the transistors must be made the same size as those in the schematic. In this tutorial the nMOS transistor uses the minimum size transistor dimensions (W = 1.5um and L = 0.6um) for the AMI C5N process. But the pMOS transistor uses the minimum size Length (.6um), but the width will be the value you have determined from your schematic simulation in lab #2.

Design rule illustrations for the AMI C5N process can be found at:
http://www.mosis.org/Technical/Layermaps/lm-scmos_scn3m.html



Schematic of Inverter
(result of lab1)



Layout of Inverter
(goal of lab 3)

Create Layout Cellview
We will assume, that you have logged on and started Cadence Design Tools, and that you already have created a design library and the schematic of the inverter.

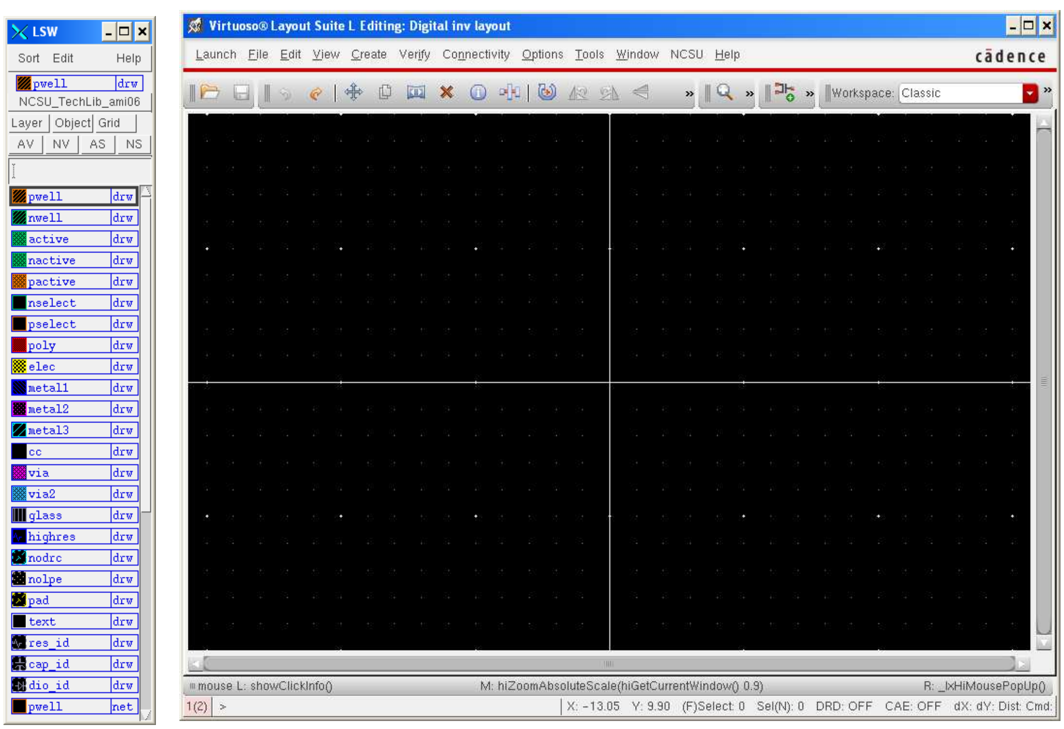
If not, please go back and perform lab 1.

STEP 1: Create a new layout view

- From the Library Manager window, Select the Digital Library, Then from the menu choose: File => New => Cellview.
- A dialog box will appear prompting you for the library, cell, and view names. Enter inv as the Cell Name and choose layout for the “TYPE”. The View Name will be automatically set to layout.

Two design windows (Virtuoso and LSW) will pop-up. The **Layer Selection window (LSW)** (small window on the left in the figure below) lets the user select different layers of the mask layout. Virtuoso will always use the layer selected in the **LSW** for editing. The **LSW** can also be used to determine which layers will be visible and which layers will be selectable. To select a layer, simply click on the desired layer within the **LSW**.

Virtuoso is the main layout editor of Cadence design tools. Commonly used functions can be accessed by pressing the buttons/icons of the toolbar on the left side of this window. There is an information line at the top of the window which shows (from left to right) the X and Y coordinates of the cursor, number of selected objects, the distance traveled in the X and Y directions, the total distance, and the command currently in use. This information can be very handy while editing. At the bottom of the window, another line shows the function of each mouse button. Note that the mouse button functions will change according to the command you are currently executing. The default mouse mode is selection, and as long as you do not choose a new mode you will remain in that mode. To quit from any mode or command and return to the default selection mode, the ‘**ESC’** key can be used.



STEP 2: Display Setup

Before drawing on a new cell you should always setup the grid properties.

- In the Virtuoso Layout Editing window, select Options => Display (or type 'e') to bring up the Display Options window shown below.
- Type in the following settings: Minor Spacing 1, Major Spacing 5, X Snap Spacing 0.15, Y Snap Spacing 0.15, then click OK. It is also very important to note that the grid spacing is in micrometers (um) and not in lambda (λ).

STEP 3: Creating VDD (Power) and GND Rails

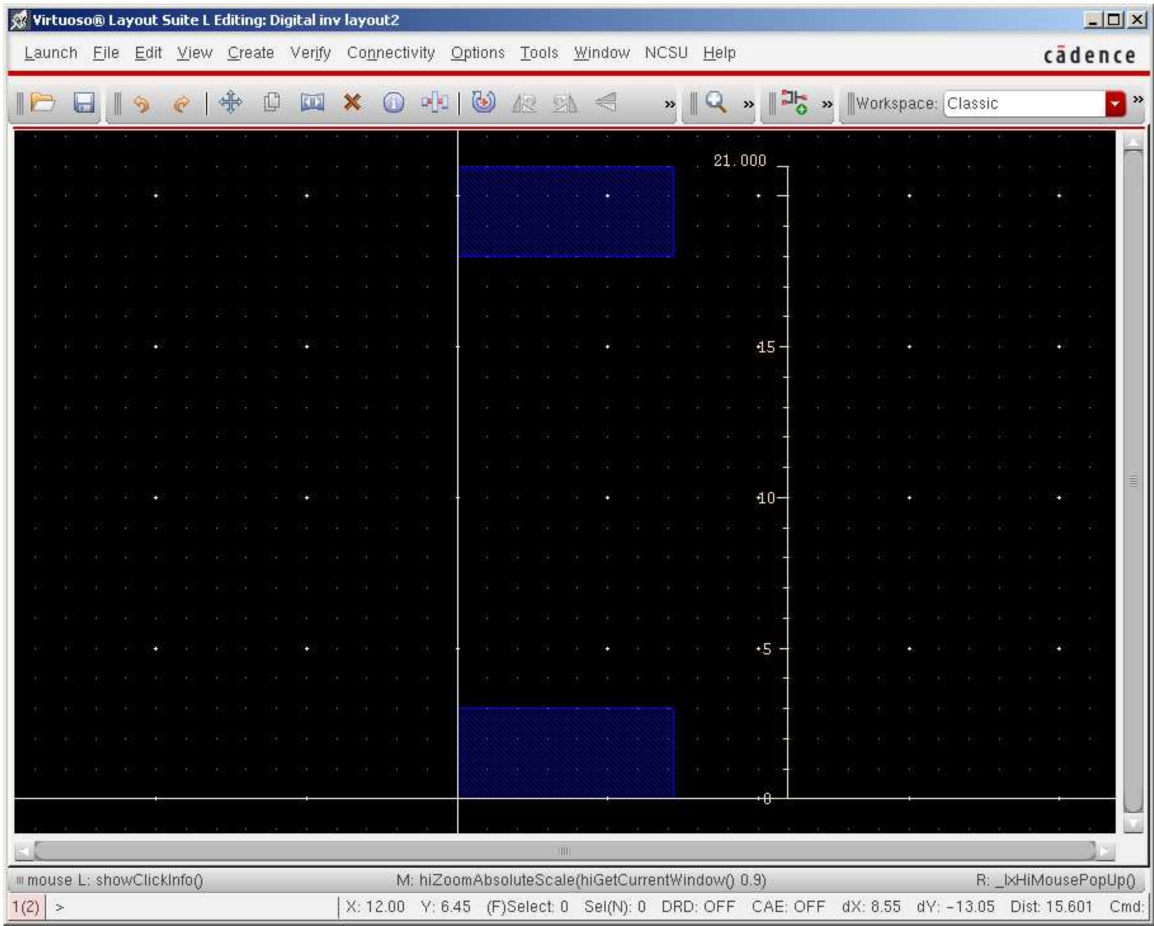
Now we are ready to start laying out our design. The first parts we will create are the power and ground rails for our inverter. Usually a circuit will consist of a large number of cells, all of which need power and ground connections. Therefore it is common to design cells with the same spacing between the power and ground so that they can easily be connected together when the cells are placed side by side. This vertical spacing is called the cell pitch and it is generally standardized for all cells in the same library to facilitate combining cells in higher-level circuits. For this tutorial the power and ground rails will be made 3um (10 lambda) wide using the Metal-1 layer and the standard cell pitch (height from bottom of the GND rail to top of the VDD rail) will be 21um (70 lambda).

Now draw the Power Rail and the Ground Rail in Metal-1 as shown below.

- Select *metal1 drw* layer from the **LSW**. In the rest of the tutorial, always use the drw layers for your layouts unless otherwise specified.
- In the Layout Editing window, press the letter "r" or select Create ->Shape -> Rectangle
- Move your mouse to the cell origin, where the horizontal and vertical guidelines intersect. Check the information bar at the bottom of the screen to make sure you are at the right location (0,0). **Click** on this point.
- Move the mouse up and right to create a rectangle. Use the data in the information bar to move your mouse to the point that is 7.2um horizontal and 3um vertical from the origin (7.2 x

3 um is always in the X direction by the Y direction, respectively). Click on this point to create the Metal-1 rectangle which will be your ground rail.

- Repeat these steps to draw the VDD rail 21um (70 lambda), top to bottom, above the GND rail. Read the ***Useful Editing Tools*** section below.



<u>Useful Editing Tools</u>

Ruler: The ruler is very useful to place objects and measure the distance between the objects.

- To start the ruler, press the letter “k” or from the menu choose: Tools->Create Ruler.
- Click the start and end point in the window; a ruler is created showing the distance between the two points.
- Hit the ‘ESC’ key to exit the ruler command.
- To clear ruler marks press <shift> k

Move: If you place the objects on the wrong place, you can use move function to adjust the location of the object.

- To begin the move process, press the letter “m” or from the menu choose: Edit -> Move
- The move dialog box will pop-up
- Click on the shape you wish to move, the move the mouse to the target location and click again. The Snap Mode is an interesting option. When this is in orthogonal setting, objects will move only along one axis. This is a good feature to help you avoid alignment problems.
- When you have finished the move operation, hit the ‘ESC’ key to exit the move command.

Stretch: If you make an object too big or too small and you wish to resize it, you can use the stretch function to adjust its perimeter.

- To begin the stretch process, press the letter “s” or from the menu choose: Edit -> Stretch
- The stretch dialog box will pop-up
- Place your mouse over (DO NOT CLICK) the edge of the object you wish to stretch. You will notice that only the edge of the object will begin to highlight.
- Once the proper edge is highlighted, click on it, then move the mouse to the place you’d like the edge to be. Click again and the edge will be set.
- Hit the ‘ESC’ key to exit the stretch command.

Copy: If you want to create the same object repeatedly, you can use the copy function.

- To begin the copy process, press the letter “c” or from the menu choose: Edit -> Copy
- The copy dialog box will pop-up
- Click in an object. Notice that an outline of the object will attach to your mouse cursor.
- Move our mouse and click when you are satisfied with the location to place a copy of the object.
- Press the ‘ESC’ key to exit the copy command.

Delete: If you want to delete an object you have drawn:

- Place your mouse over the object and left-click to select it.
- Press the Delete key on the keyboard.
- Press the ‘ESC’ key to exit the delete mode

Undo: When you make a mistake (accidentally delete a component, etc.), you can undo the action by pressing the “**u**” key or clicking on the Undo icon in the toolbar. To “REDO” something you have just ‘undone’ you may press the uppercase “**U**” key.

Zoom In Window: If you wish to enlarge a small area of your drawing, press the letter “**z**” then click in the left most area you wish to enlarge and release, then click on the right most bottom of the area you wish to enlarge (you will notice a square is drawn around the area you’d like enlarged.

Zoom Full: If you wish to see the entire drawing area, press the key: “f” for full view.

STEP 4: Draw an nMOS Active Layer

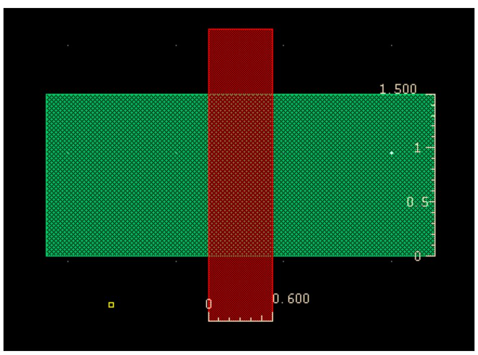
Now we need to add an nMOS transistor to the layout of the CMOS inverter. Normally the pMOS transistors are at the top near the VDD rail and the nMOS transistors are at the bottom of the layout near the GND rail. From the schematic we know that the nMOS transistor has a channel width of 1.5um. The width of the transistor (W) will correspond to the width of the active area. We want to draw a horizontal transistor so the channel width will be measured top-to-bottom of the active layer (Y-dimension of the information bar).

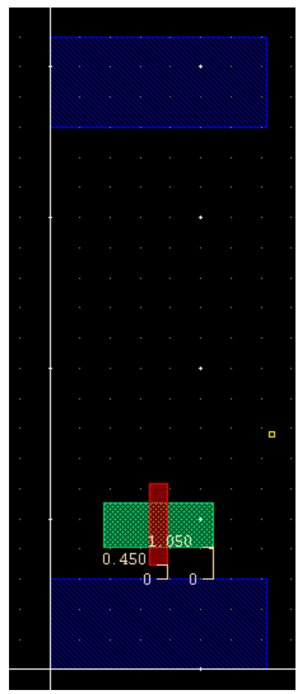
- Select ***nactive*** layer from the LSW.
- In the Layout Editing window, press the letter “r” or select Create ->Shape -> Rectangle
- Draw a rectangle that is 3.6um x 1.5um. Place the left bottom corner of the box at (1.8, 3.9) and click once. Then move the cursor to (5.4, 5.4) and click again.

STEP 5: The Gate Poly

We will use a vertical polysilicon rectangle to create the gate of the nMOS transistor. Note that the length of the transistor channel (L) will be determined by the width of this poly rectangle.

- Select poly layer from the LSW.
- In the Virtuoso Layout Editing window draw poly rectangle that is 0.6 x 2.7 um over the center of the nactive as shown in the figure below. Start drawing the poly rectangle 1.5um from the left side and 0.6um above the top of the active layer.

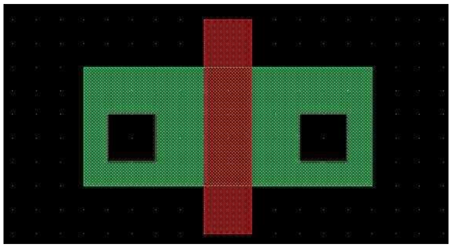




STEP 6: Making Active Contacts

Active Contacts provide a connection between the Metal-1 layer and the Active layer, which in this case is the drain and source regions of the nMOS transistor.

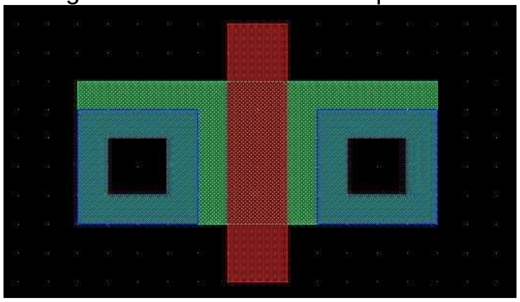
- Select the **cc** layer from the LSW.
- In the Virtuoso Layout Editing window draw a box that is 0.6x 0.6 um within the active area.
- Start drawing the contact at 0.3um away from the bottom-left corner of the nactive layer.
- Draw the second contact on the right side of the nactive layer as shown below. As set by the design rules, the contacts must be at least 0.3um from the edge of the active layer. You might want to use the Copy command (see Useful Editing Tools section above) to simplify this procedure.



STEP 7: Covering Contacts with Metal-1

The Active Contact layer defines where a hole will be formed in the oxide that separates the active region from the Metal-1 layer. To complete the contact, we must ALWAYS cover the contact with a Metal-1 layer.

- Select layer Metal-1 from the LSW.
- In the Virtuoso Layout Editing window draw a 1.2um square to cover each contact.

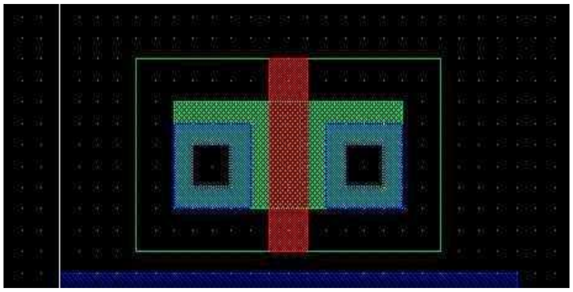


Note: Metal-1 must extend over the contact in all directions by at least 0.3um (1 lambda).

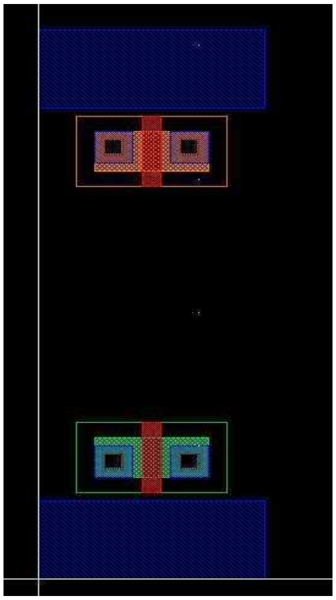
STEP 8: Create N-Select Layer

Each diffusion (active) area must be specified as being of n-type or p-type. This is accomplished by a defining the window of n-select (or p-select) around each n-type (or p-type) transistor. Since we are making an nMOS right now, we will choose the nselect layer.

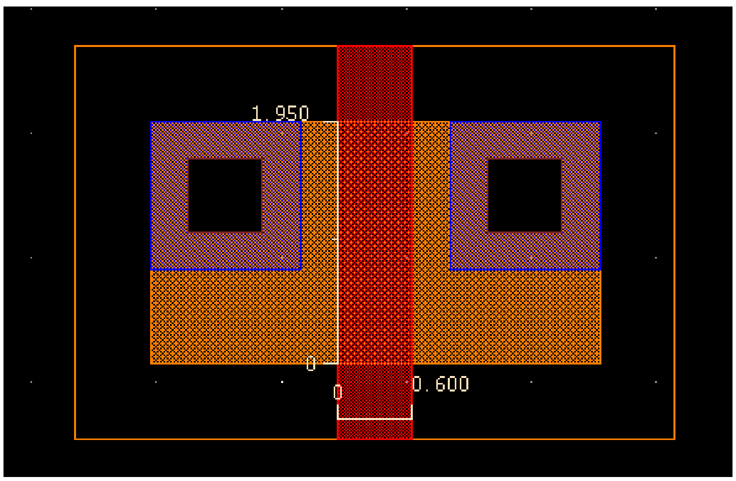
- Select nselect layer from the LSW.
- Draw a rectangle extending over the active area by 0.6um (2 lambda) in all directions.
- This completes the nMOS transistor, which should look like the following figure.



STEP 9: Drawing PMOS
Repeat steps 4-8 to make a pMOS transistor at the top of your cell, just below the VDD power rail. The only difference between drawing nMOS and pMOS is that you will be using pactive and pselect layers in place of the n-type layers specified in steps 4-8. Place the pMOS active the same distance from the VDD rail as your nMOS active was from the GND rail.



How to set the Width of the transistor:



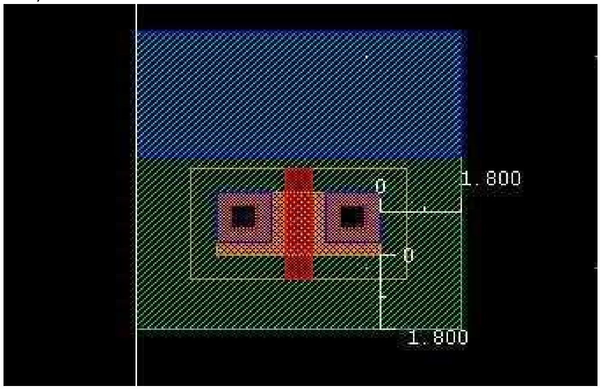
In this picture, the length of the PMOS=.6 and the width=1.95

You will keep the length the same, but change the width to the value you determined in lab 2's parametric simulation.

STEP 10: Drawing the N-Well

The selected process, AMI C5N, uses a p-type substrate, where nMOS transistors can be formed, and requires an n-well, where pMOS transistors can be formed. This n-well. We must add an n-well to our cell, which will be the effective substrate (body terminal) for pMOS transistors.

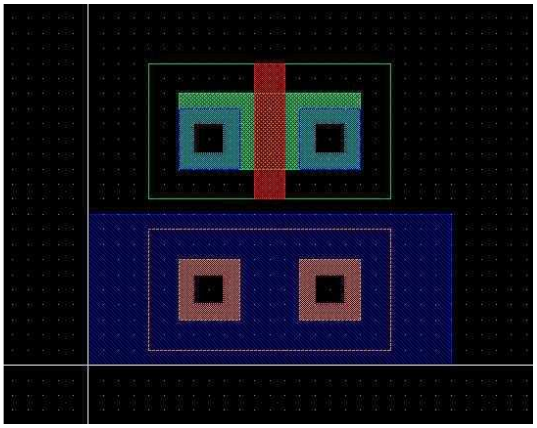
- Select the nwell layer from the LSW.
- Draw a large n-well rectangle around pactive area. The n-well must extend over the pMOS active area by a large margin, at least 1.8um (6 lambda). Align the top side of the nwell to the top of the VDD rail, as shown below.

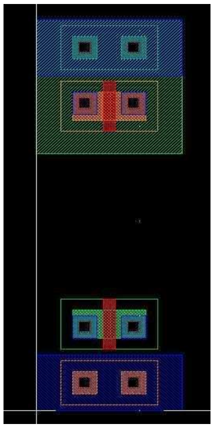


STEP 11: Create Substrate/Well Contacts (plugs)

The body terminals of the nMOS and pMOS transistors are the substrate and n-well, respectively. These terminals must be tied to the proper supply rail, substrate to GND and n-well to VDD. To simplify this connection, we can place Active Contacts directly on the existing supply rails. This will require adding active, contact, and select layers on top of the existing metal-1 layer as shown in the figure below.

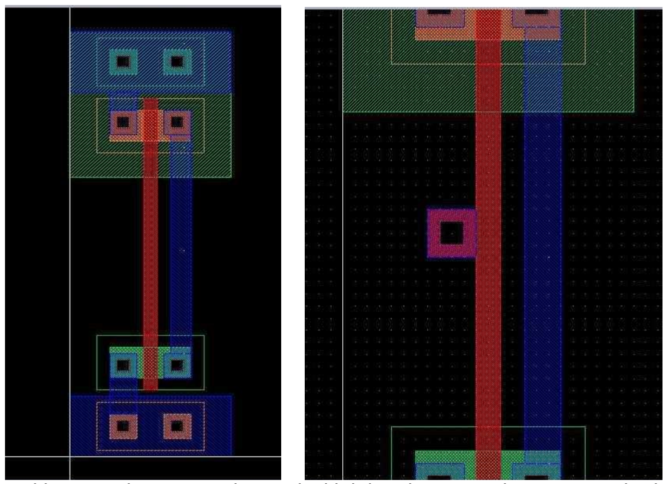
- Select the **pactive** layer from the LSW
- Draw a 1.2um x 1.2um square placed in the center of the GND rail directly beneath the Active contact on the nMOS transistor. Repeat to add a contact beneath the second nMOS active contact.
- Select the cc layer from the LSW and 0.6um x 0.6um contacts inside the pactive squares.
- Select **pselect** layer from the LSW and draw a box extending over both pactive squares by 0.6um on each side.
- Repeat this process using complementary layers (nactive, nselect) to add n-type active contacts to the VDD power rail.
- Notice the active contacts on the GND rail are p-type since they connect to the p-type substrate and they are n-type on the VDD rails since they connect to the n-type n-well. If we were to switch these layers we would make diodes rather than ohmic (low resistance) contacts.





STEP 12: Connect Transistors Nodes to Match Schematic and Form the Inverter

- Select poly layer from the LSW.
- Draw a rectangle to connect the poly at nMOS and pMOS.
- Note: To connect polygons of the same layer (eg., poly) you simply need to add another polygon that makes contact to each of the original layers. If the layers touch or overlap, they will form a continuous connection.
- Select layer Metal-1 from the LSW.
- Draw a rectangle to connect the source of the nMOS to GND rail. In this tutorial, the left side of the MOS is the source, and the right side is drain.
- Draw a rectangle to connect the source of the pMOS to VDD rail.
- Draw a rectangle to connect the drains of the nMOS and pMOS transistors. This is the inverter output node.



(left) Connected input and output nodes and (right) Poly-to-Metal contact on the inverter input.

STEP 13: Make All I/O Nodes Available in Metal-1

As a standard practice that will help when connecting multiple cells (gates), we need to ensure that all of our input and output nodes have a connection in Metal-1. For our inverter, the output is already in Metal-1, but the input (the node that links the gates of both transistors) is only in poly. We will make a connection to Metal-1 on the input by adding a poly-to-metal contact.

- Draw a 1.2 x 1.2 um square of poly extended from the existing poly away from the output metal (see figure below).
- Add a contact (0.6um x 0.6um square in the cc layer) in the center of the new poly square.
- Draw a Metal-1 square (about 1.2 x 1.2 um) that overlaps the poly box.

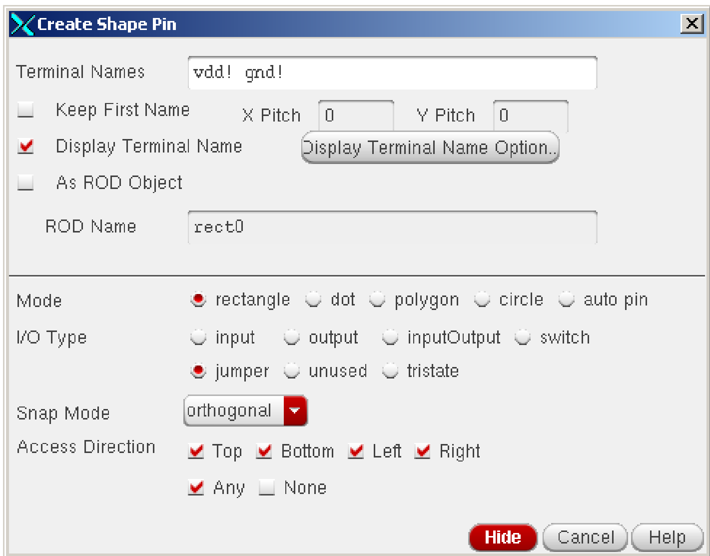
STEP 14: Add Pins to the I/O Nodes

Now we need to assign pin names to the power, input, and output nodes.

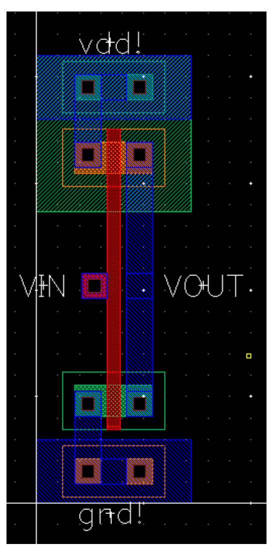
- From the LSW, select the layer: ***metal1***
- In the Virtuoso Layout Editing window select **Create -> Pin** to open the *Create Shape Pin* window. Using this window we will first set the global power pins then the input and output.
- In the Terminal Names field, enter **vdd! gnd!** which are the names of the two global power pins. Put both names in this field, separate by a space, and be sure to include the '!'.
- Check **Display Terminal Name**. In I/O Type select **jumper**.
- In the Virtuoso Layout Editing window, move the mouse over the VDD rail of the inverter. Be sure to place your mouse over metal-1 layer and not other layers (e.g., active) on the VDD rail. Click any place inside the VDD rail, release, move your mouse, and move it to create a small box. Then click again to place the pin. Click a third time to place the label: vdd!.
- Now move the mouse to the GND rail, place the gnd! pin the same way you placed vdd!. Note that because you entered both names (vdd! and gnd!) as Terminal Names, you can

place both the same order you entered the names. You can use this same procedure to place multiple pins OF THE SAME TYPE (power/jumper, input, output).

- In the LSW, select the poly layer
- Go back to the Create Shape Pin window and create an input pin with name: **VIN** in the Terminal Names field. Change the I/O Type to **input**.
- In the Virtuoso Layout Editing window, move the mouse over the middle of the input poly layer and place the pin.
- In the LSW, select the metal1 layer again
- Repeat the pin creation process to place the output pin on the output **metal1**. Use **VOUT** in Terminal Names and **output** in I/O Type.
- Note: The pin names in your layout must match the pin names in your schematic (in case you didn't use VIN and VOUT as your pin names). However, power rails must have the names: vdd! and gnd!



- Now we have the final layout of an inverter! See figure below.



Useful skill: As layouts get more complex, you may find it useful to view only specific layers rather than all of them. This will allow you to see exactly what layers are present which can be difficult when many layers are placed on top of each other. Here's how this is done.

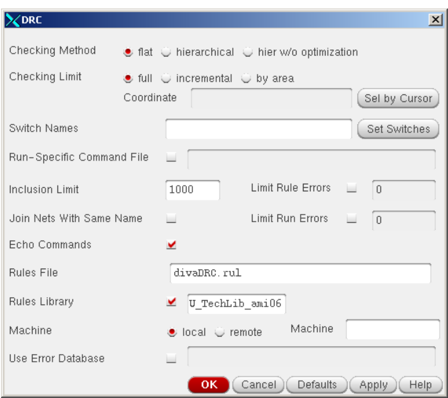
- From LSW select Edit Set Valid Layers.
- Select the box on the right side of the layer(s) you want view in the layout. For example, to view only "metal1 pn" select the box on the right side of metal1 pn. Press OK and only the selected layers will be shown in the Virtuoso Layout Editing window.
- To make all layers visible again, press the AV button on the LSW.

Design Rule Checking

Layout must be drawn according to strict design rules. After you have finished your layout, an automatic program will check each and every polygon in your design against these design rules and report violations. This process is called Design Rule Checking (DRC) and MUST be done for every layout to ensure it will function properly when fabricated.

Note: You are STRONGLY advised not to wait until your layout is completed to check for design rule violations. In future layouts, run DRC frequently as you add layers to your cell. If you wait until you are finished to check for errors, it will be much hard to track down and fix all your errors.

- In the Virtuoso Layout Editing window select Verify => DRC. This will open the DRC options dialog box. The default options for the DRC are adequate for most situations.
- Click OK to start DRC. DRC results and progress will be displayed in the CIW (Command Interpreter Window) (the main window when you start Cadence).



(left) DRC dialog window and (right) CIW showing DRC results.

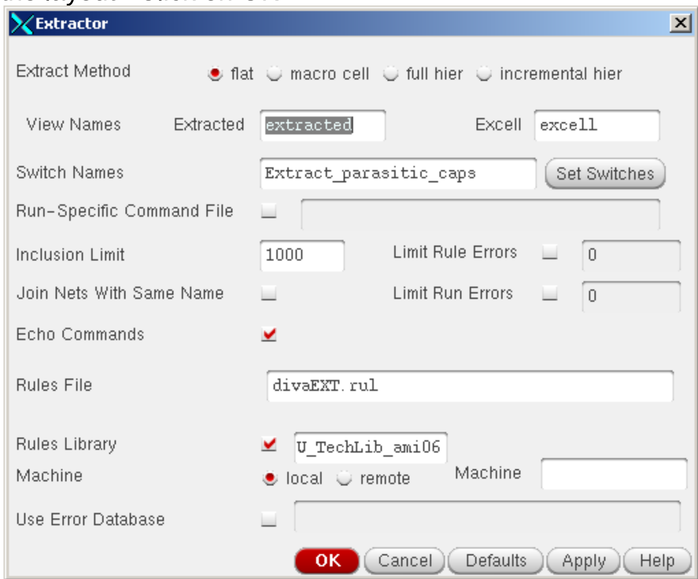
- After the DRC is complete, the bottom line in the CIW will show "# Total errors found". If the number is greater than zero, any errors will be highlighted on the layout. Using the design rules as a guideline, correct all errors and perform another DRC until you get no errors.
- The DRC will be successful when you see the results saying "0 Total errors found", as shown above.

Layout Parameter Extraction

The mask layout you've created contains only physical data. In fact it just contains coordinates of rectangles drawn in different colors (layers). The extraction process identifies the devices from the layout and generates a SPICE-like netlist and other files necessary to complete the design process.

Before beginning a layout extraction you must have the cell opened in the layout window and the layout should have already passed DRC.

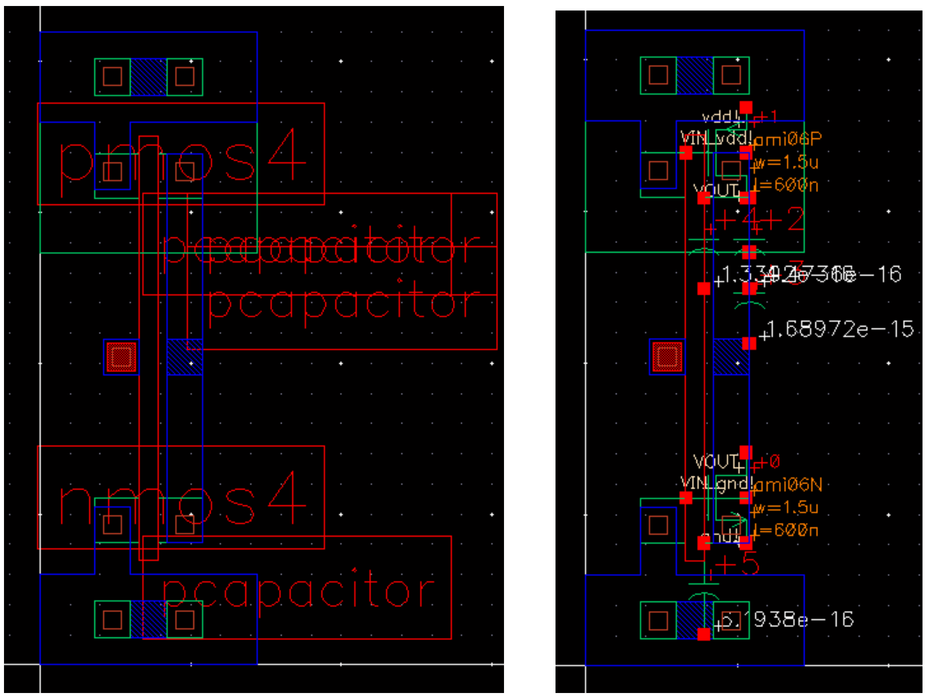
- In the Virtuoso Layout Editing window select Verify -> Extract. A new window (below) with extraction options will appear.
- Click on Set Switches and select **Extract_parasitic_caps**. This setting will extract parasitic elements from the layout. Click on OK.



- After extraction check the Command Interpreter Window to make sure there are no errors.
- Following a successful extraction you will see a new cell view called **extracted** added to the Library Manager window.

The Extracted Cell View

- Open the extracted cellview from the Library Manager window. This will open up a layout that looks almost identical to the layout you produced earlier.
- You will notice that only the I/O pins appear as solid blocks and all other shapes appear as outlines. The red rectangles indicate that there are a number of instances (electrical elements) within this hierarchy.
- Try pressing 'Shift+F' to view the complete hierarchy. A number of symbols are revealed. If you zoom in, you will be able to identify individual elements such as transistors and capacitors. You will notice that the parameters (e.g. channel dimensions) of these devices represent the values as they were drawn in the layout view.
- Verify that the transistors extracted from your layout match in width and length (1.5 x .6um) by zooming in and looking at the transistor devices.

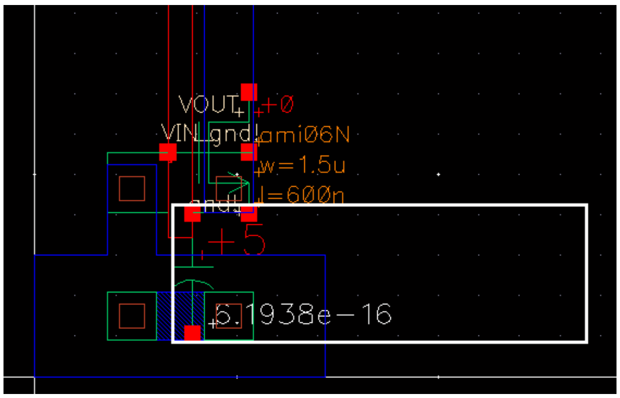


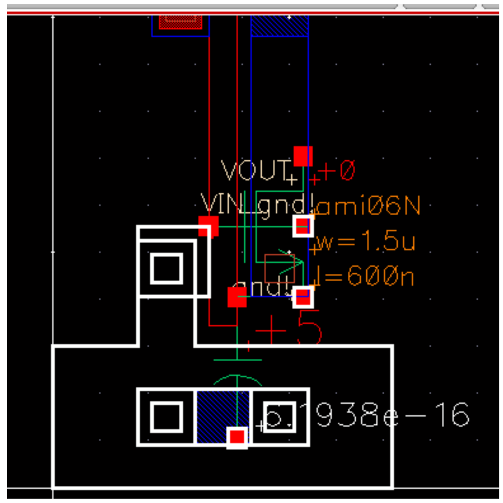
Extracted view (left) before and (right) after showing extracted devices.

In addition to the actual transistors you will notice a number of elements (mainly capacitors) in your extracted cell view. These are not actual devices. They are parasitic capacitances, which are side effects formed by different layers you used for your layout.

Examining the Parasitics

- Zoom in on the bottom most parasitic capacitor as shown in the figure below.
- It will be approximately 6.19 x 10^{-16} Farads. A very small parasitic.
- Click on the outline of the substrate body contact (as shown in the figure on the right below)
- Notice the bottom pin of the parastic capacitor "lights up"
- This means that the body contact has a parasitic capacitance associated with it. Click on other parts of the layout to see where the top terminal of the capacitor is.



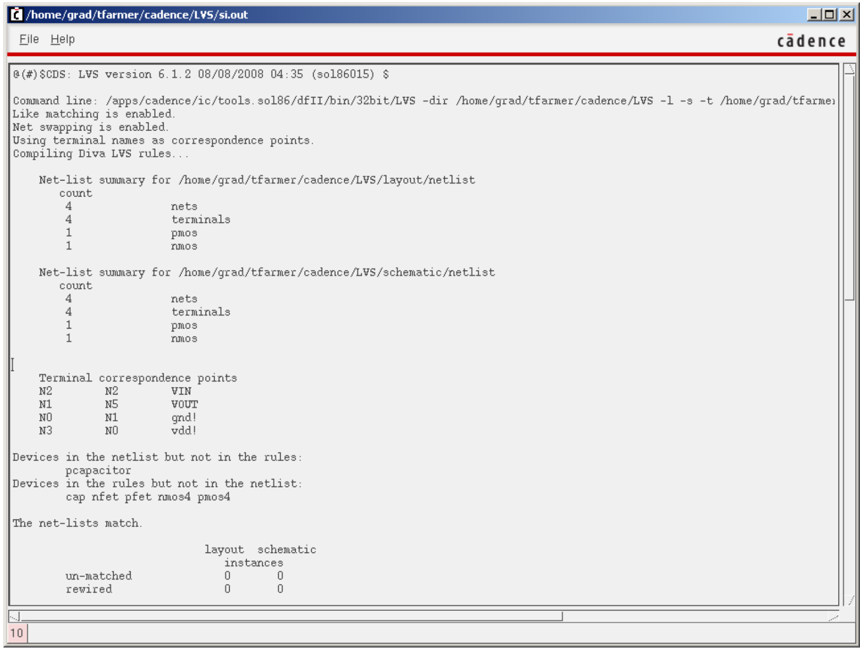


Layout vs. Schematic Comparison
The next step is to compare the netlist extracted from the layout with the schematic to ensure the layout you have drawn is an identical match to the cell schematic.

- In the Virtuoso Layout Editing window select Verify => LVS to open the LVS window.
    - o If you had previously run an LVS check, this would open a small warning box. Make sure that the option Form Contents is selected in this box and click OK.

- The top half of the LVS options window is split into two parts, schematic and extracted.
- Make sure that the entries in the Library, Cell, and View boxes are correct for your circuit.
- Select Run to start the comparison. The comparison algorithm will run in the background, the result of the LVS run will be displayed in a message box. Be patient, even for a very small design the LVS run can take some time (minutes).
- When the LVS comparison is complete you will get a pop up window saying "Job . . . has succeeded". This does NOT necessarily mean the circuits match, just that the LVS operation is complete. Click OK to close this window.
- In the LVS window, click on the Output button (just right of the Run button) to display the LVS result. Scroll through this window and take a look at the LVS result. The most important part of the report tells if errors were found or if netlists did match ("The netlists match" as shown below).
- If there are no errors, your layout is complete and correct. If there are errors, you will have to reload the layout view, fix the problems, and re-run LVS until there are no errors.

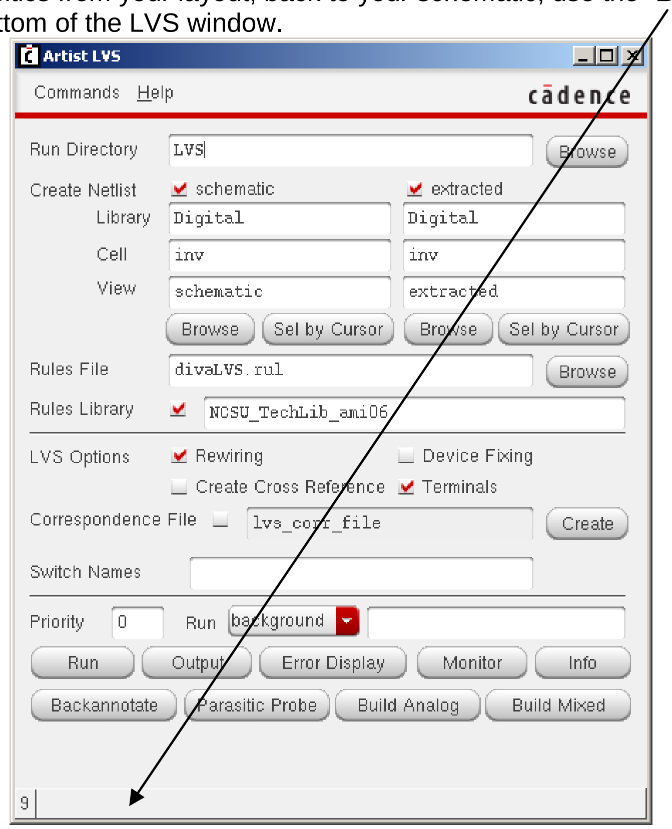
Some of the other options in the LVS window are for finding mismatches between two netlists and for generating netlists that include only parasitic effects relevant to one part of the circuit. Feel free to explore these options to learn more about the Cadence tools.


/home/grad/tfarmer/cadence/LVS/si.out
File Help
cādence
@(#)$CDS: LVS version 6.1.2 08/08/2008 04:35 (sol86015) $
Command line: /apps/cadence/ic/tools.sol86/dfII/bin/32bit/LVS -dir /home/grad/tfarmer/cadence/LVS -l -s -t /home/grad/tfarme
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...
Net-list summary for /home/grad/tfarmer/cadence/LVS/layout/netlist
count
4 nets
4 terminals
1 pmos
1 nmos
Net-list summary for /home/grad/tfarmer/cadence/LVS/schematic/netlist
count
4 nets
4 terminals
1 pmos
1 nmos
Terminal correspondence points
N2 N2 VIN
N1 N5 VOUT
N0 N1 gnd!
N3 N0 vdd!
Devices in the netlist but not in the rules:
pcapacitor
Devices in the rules but not in the netlist:
cap nfet pfet nmos4 pmos4
The net-lists match.
layout schematic
instances
un-matched 0 0
rewired 0 0
10

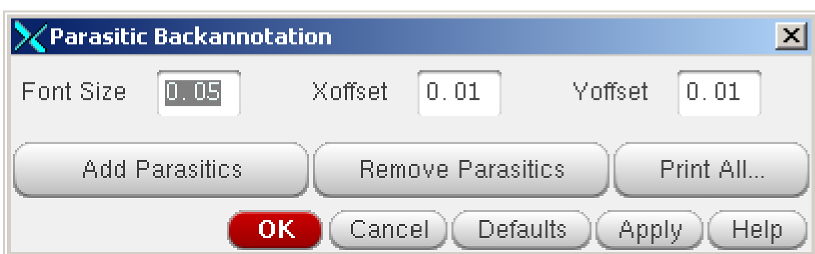
BackAnnotating Parastics:

In your inverter *schematic*, the wires and interconnects are ideal. They do not take into account any parasitic capacitances that may exist due to your layout. In this simply inverter layout, you will have some parasitics, but in more complex designs, you most certainly will many that will affect your simulation results (timing, voltage levels, etc).

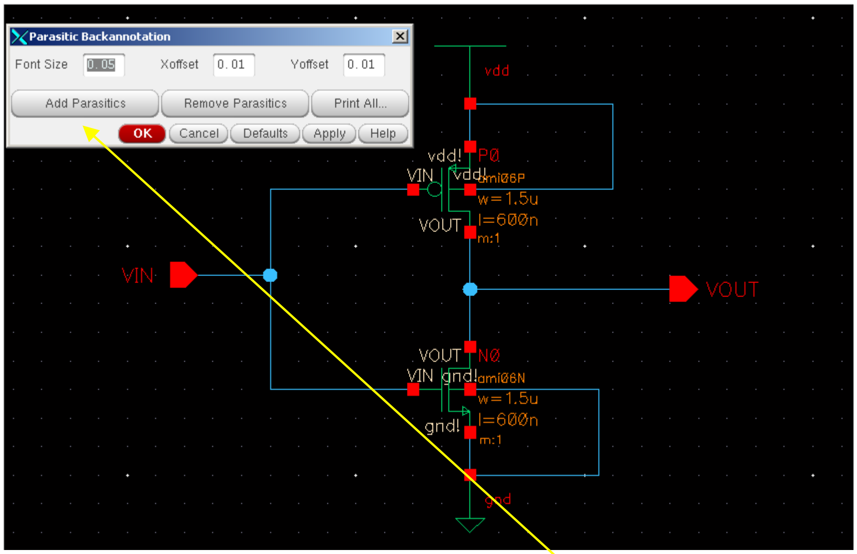
- To add the parasitics from your layout, back to your schematic, use the "**Backannotate**" button on the bottom of the LVS window.



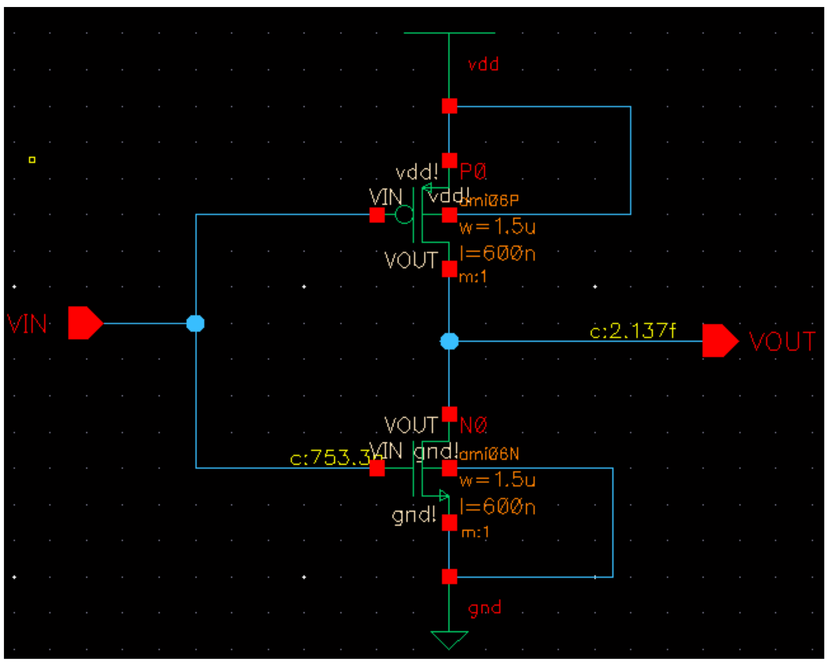
- Next you will see the following window come up:



- Before pressing "Add Parasitics" open up the schematic for your inverter from the Library Manager as shown below.



- Once the schematic window is open, click on the “Add Parasitics” button in the dialog box
- If successful, you schematic should now updated with the parasitics from your layout as in the figure below:



- Notice the 2.137fF parasitic on the VOUT, and 753.3aF parasitic on the VIN.
- Check and save this back annotation
- Then resimulate with Spectre to see if this has affected your transient simulation of your inverter.
- This schematic now incorporates the parasitic results of your layout. If you change your layout, you must reextract and rebackannotate to update the schematic with any new parasitics. Your goal is of course to always layout your device in such a way that you have as small a set of parasitics as possible.