The George Washington University
School of Engineering and Applied Science
Department of Electrical and Computer Engineering
ECE 20 – SPICE Tutorial 5

Designing a Common-Emitter Amplifier

Background:

There are 2 popular types of Common-Emitter amplifiers:

1. Common-Emitter Amplifier without emitter degeneration (Fig 1.1)
    - sometimes called: *grounded emitter,* or simply*: common-emitter*
    - This is the type you built in lab 5
2. Common-Emitter Amplifier with emitter degeneration (Fig 1.2)
    - sometimes called: ***common-emitter with emitter resistor***
    - There are 3 configurations of this circuit possible:
        a. Non bypassed emitter resistor
        b. Bypassed emitter resistor with a series external emitter resistor
        c. Bypassed emitter resistor with a parallel external emitter resistor

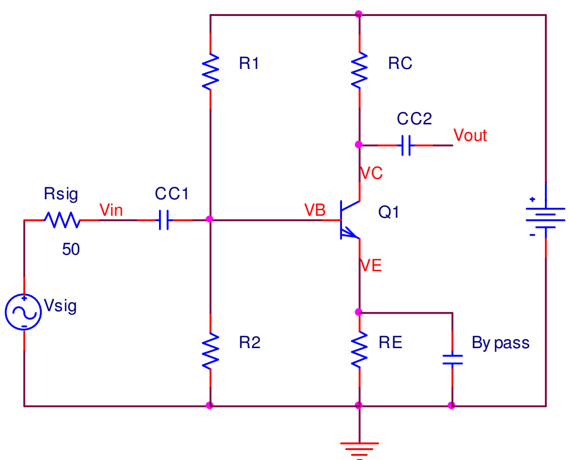


Fig 1.1 - C.E. without emitter degeneration

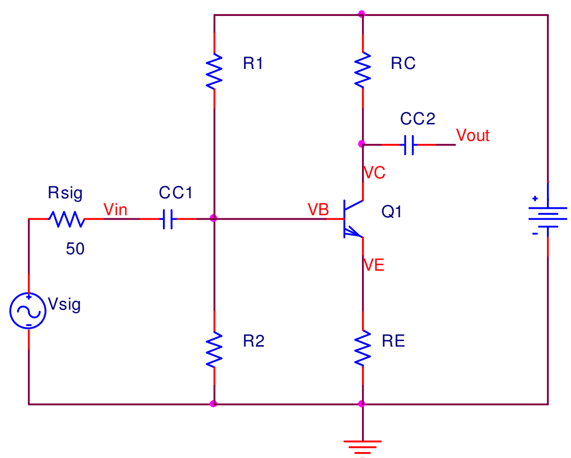


Fig 1.2 - C.E. with emitter degeneration (no bypass cap)

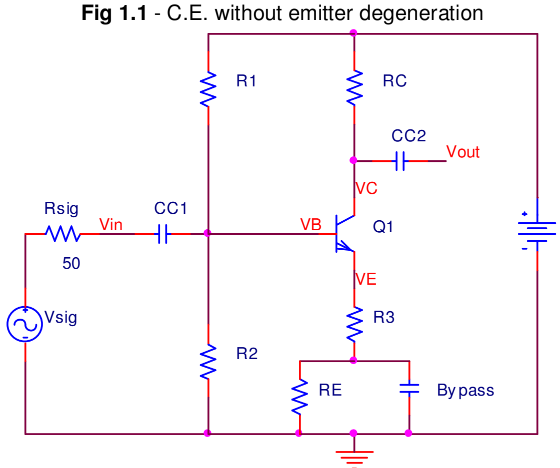


Fig 1.3 - C.E. with emitter degeneration series resistor

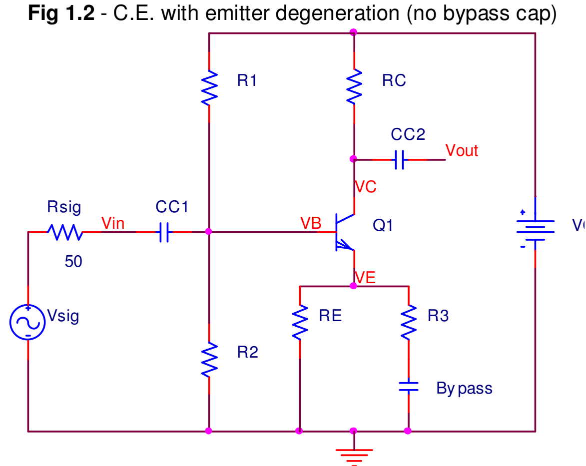


Fig 1.4 - C.E. with emitter degeneration parallel resistor

The 2 forms of the common-emitter amplifier and their various configurations have own advantages and disadvantages when compared to one another. From the perspective of this tutorial, we will concentrate on the way 'gain' is controlled for each of the circuits. But, no matter the configuration, for any common-emitter amplifier, **the *input* signal is always through the *base* terminal, the *output* is always take from the *collector* terminal, and the emitter is always 'common' to both the input and output.**

For type 1 (C-E without emitter degeneration), from figure 1.1 the 'bypass' capacitor shorts the **emitter** to **ground** for high frequency signals; hence the name 'grounded emitter.' This amplifier is discussed in Sedra p 467-470. The voltage gain of this amplifier (when no load is present) is A_V=-g_mRC. The designer can only control the value of RC (and to some extend g_m) to control the voltage gain of the amplifier. This is the type you built in lab 5 during the common-emitter portion of the lab.

For type 2a (C-E with emitter degeneration – non-bypassed emitter resistor), shown in figure 1.2 there is no 'bypass' capacitor. The emitter terminal is 'common' to both the input and output through the resistor connected to the emitter (RE). The emitter resistor (RE) serves to give bias stability to the circuit. This amplifier is discussed in Sedra p 470-474. The gain of this amplifier (when no load is present) is A_V= -alpha RC / (re + RE) or more simply: Av ≈ - RC / (re + RE). The designer can now use RC and RE to control the voltage gain of the amplifier.

For type 2b (C-E with emitter degeneration – bypassed emitter resistor with series emitter resistor-R3), shown in figure 1.3 the 'bypass' capacitor shorts the resistor R3 to ground for high frequency signals. The emitter terminal is 'common' to both the input and output through the resistor (R3). The emitter resistor (R3) serves to give bias stability to the circuit. This amplifier is not discussed in Sedra. The gain of this amplifier (when no load is present) is Av ≈ - RC / (re + R3). The designer typically leaves RC and uses R3 to control the voltage gain of the amplifier.

For type 2c (C-E with emitter degeneration – bypassed emitter resistor with parallel emitter resistor-R3), shown in figure 1.4 the 'bypass' capacitor shorts the resistor R3 to ground for high frequency signals. Typically R3 is much smaller than RE, making it so RE is 'bypassed' by comparison to R3. R3 is an easier 'path to ground' than for AC signals. The emitter terminal is 'common' to both the input and output through the resistor (R3). This amplifier is not discussed in Sedra. The gain of this amplifier (when no load is present) is Av ≈ - RC / (re + R3). The designer typically leaves RC and uses R3 to control the voltage gain of the amplifier. The advantage of this design is that R3 serves no purpose in the 'DC biasing' of the amplifier. So the designer only sets the value of R3 after the 'DC bias' has been determined for the amplifier.

The student is encouraged to use any of the common-emitter amplifier configurations show above in labs and projects. Because type 2 is stable, is the easiest to 'bias,' and then to tailor the 'gain' without affecting its DC bias, it will be covered in this tutorial.

Designing a Common-Emitter Amplifier w/ emitter degeneration through a parallel emitter resistor

Problem: Design a Common-Emitter Amplifier using the 2N3904 transistor that meets the following specifications:

IC = 2mA
VCC = 30 Volts
Av (without load) = -50
Rin (DC) = 4KΩ
RL = 1KΩ
v*in* = 10mV @ 10kHz

Step 1) Begin with the skeleton of the amplifier we'd like to design, figure 2.1:

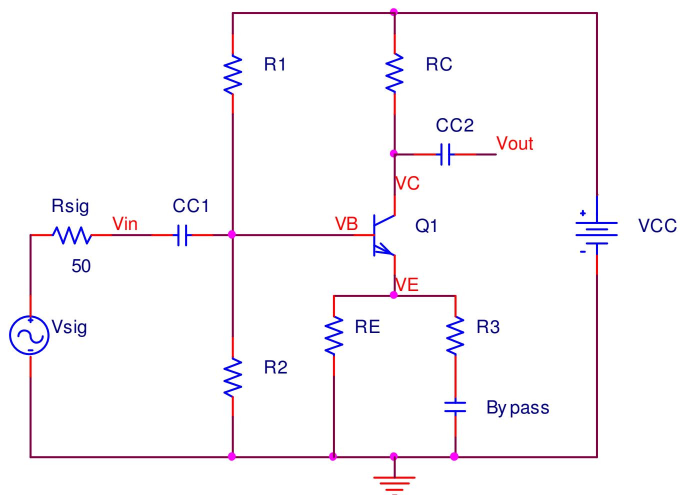


Fig 2.1 – Complete Common-Emitter Amplifier

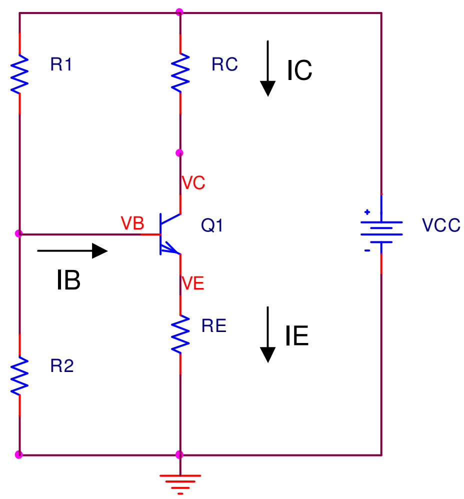


Fig 2.2 – C.E Amplifier (DC only)

- Our goal as designers will be to determine values for RC, RE, R1, R2, R3, CC1, CC2, and the Bypass Cap based on the specs given. We begin by determining the values of RC, RE, R1, and R2 to provide DC bias to the transistor. Then we view the circuit from an 'AC' perspective to determine the size of R3 to set the 'gain' for the amplifier.

- From a DC perspective, the amplifier looks like the circuit in figure 2.2. This is because the impedance of the CC1, CC2, and Bypass capacitor at DC (≈ 0 Hz), is nearly 'infinite.' So the capacitor's look like 'open' circuits at DC. This is why R3 disappears from the circuit.

- Fig 2.2 looks just like what we did in Lab 5, except we're solving the problem in reverse.

Step 2) Determine the value of RC

- Because we take the 'output' voltage from VC, we start with the equation for VC:
- Due to the equation: VC = VCC – IC * RC (which is just Ohm's law for the voltage across RC),
- The maximum output voltage we can have when IC = 0mA, is 30Volts (VCC). The minimum output voltage we can have when IC is at its highest, which makes VC = 0 Volts. We want the 'AC' signal that comes out to 'swing' symmetrically around the mid-point (½ VCC).

We set **VC** = ½ (VCC) = **15V**

- Since IC is given at 2mA, we can use Ohm's Law, to determine RC:

$$RC = \frac{(VCC - VC)}{IC} = \frac{(30-15)}{2mA} = 7.5K\Omega$$

Step 3) Determine the "Q" point of the transistor

- From the test bench we created in lab 4 to characterize the 2N3904 transistor, we perform a parametric sweep simulation to obtain the IV curve for the transistor. We sweep VCE from 0 to VCC (30V). I have swept current IB from 0 to 20uA, in steps of 2.3uA. I used trial and error until I was able to get a curve to tell me what IB was, when IC=2mA.

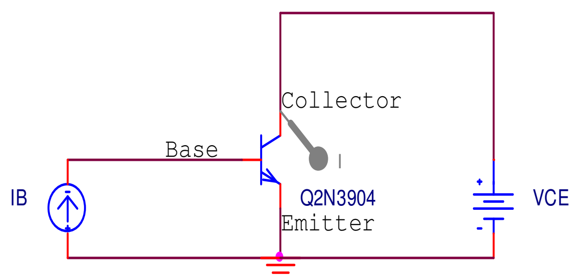
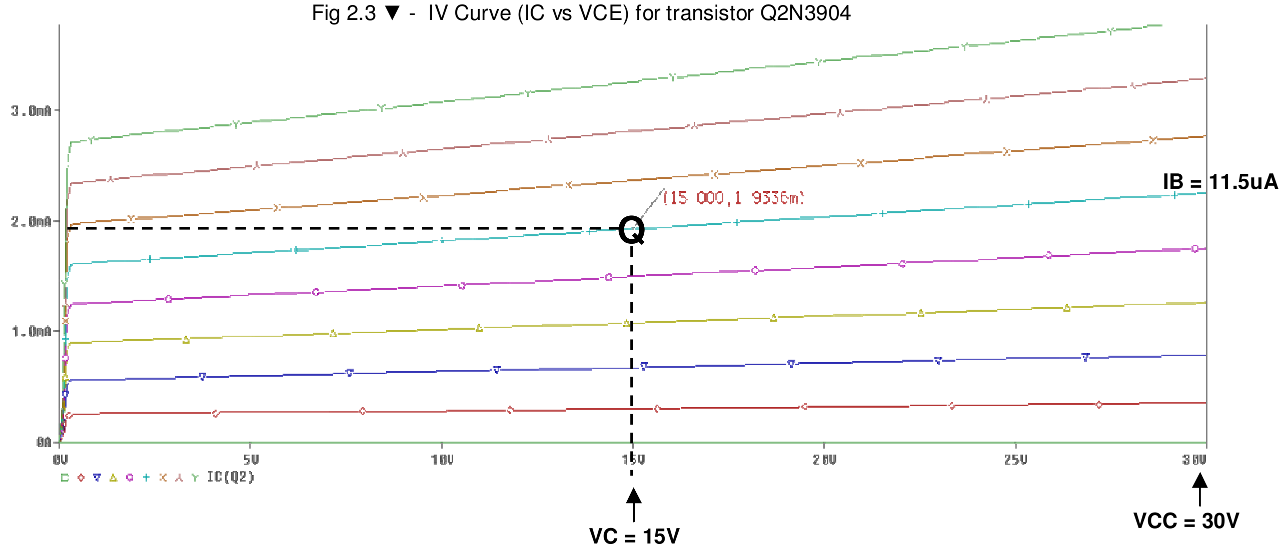


Fig 2.3 ▼ - IV Curve (IC vs VCE) for transistor Q2N3904



- In the spec, we were told IC = 2mA. We determine that VC = 15V in the last step. That is our 'quiescent value' or Q value. From the IV-Curve, we can see that the 2N3904 transistor will supply ~2mA of current when the base current is set to IB=11.5uA. With this information, we can determine IE, R1, R2, and RE. So far we know:

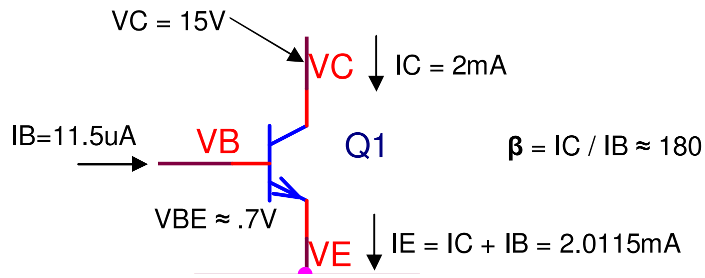


Fig 2.4 – DC Bias State for the 2N3904

Step 4) Find RE, VE, VB:

- For this type of common-emitter amplifier, as a rule of thumb, we choose RE to be 10% of RC

RE = 10 % RC = (.1 * 7.5KΩ) = **750 Ω**

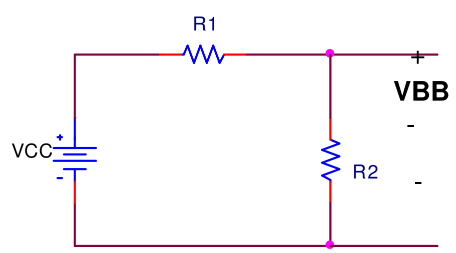
- From Ohm's Law, we can find VE:

VE = IE * RE = 2.0115mA * 750 Ω ≈ **1.5V**

VB = VE + VBE = 1.5 + .7V = **2.2V**

Step 5) Use VCC, VB, IB & RIN (DC), to find R1 & R2:

- Our goal is to deliver 11.5uA to the base of the transistor
- R1 & R2 must be properly sized to achieve this goal
- We generate 3 equations to find R1 & R2
- Since R1 & R2 are in parallel (as we learned from lab 5's tutorial), we know:



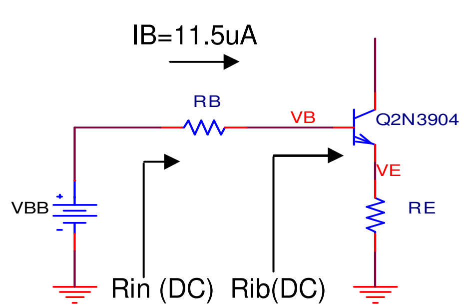
The Thevenin Voltage (VBB) is:

Eqn 1: $$VBB = VCC\left(\frac{R2}{R1+R2}\right)$$

The Thevenin Resistance (RB) is:

Eqn 2: RB = R1 || R2

- Using the Thevenin equivalent resistance (RB) for R1 & R2 (as we did in lab 5), we know our circuit can be redrawn to look like this:



Using Ohm's Law, we generate eqn 3:

$$\left(\frac{VBB-VB}{RB}\right) = IB$$

Eqn 3: $$VBB = IB * RB + VB$$

- In equations 1-3, we know VCC, IB, and VB. But we do not know R1, R2, RB, or VBB. That's 4 unknowns, but only 3 equations, we need to find one of these variable's value to solve them all. We can use the spec value for Rin(DC) to find the value of RB.
- From the Thevenin equivalent figure above, we can see that:

Eqn 4: Rin(DC) = RB || Rib(DC)

- Rib(DC) is the input resistance looking into the 'base' of the transistor. Since only RE is attached to the emitter at DC (because R3 + C bypass appears as an infinite load at DC), we can use the value found in Sedra (in the common-emitter with emitter resistance section - p 472) for Rib:

$$Rib = (\beta + 1)(re + RE)$$

We know from Sedra (p459), that:

re = VT / IE = .026V / 2.0015mA ≈ 13Ω

This makes Rib ≈ 138Ω

- Using Rib, and Rin, from equation 4, we can solve for RB:

$$RB = \left(\frac{Rin(DC) * Rib(DC)}{Rib(DC) - Rin(DC)} \right) \approx 4K\Omega$$

- With RB found, we can use ***equations* 1, 2, and 3** (+ some Algebra) to find R1 & R2:

R1 ≈ 53KΩ
R2 ≈ 4KΩ

- All the 'biasing' resistors, currents, and voltages have now been found!

Step 6) Use R3 to set the gain for the CE amplifier

- The gain for this type of common-emitter amplifier is (with no load attached):

$$Av(unloaded) = -\left(\frac{RC}{re + R3} \right)$$

- The spec requires Av (unloaded) to be equal to -50, which makes R3:

$$R3 = \left(\frac{RC}{Av(unloaded)} \right) - re = 137\Omega$$

Step 7) Determine the gain when load is attached:

- The gain for this type of common-emitter amplifier (with a load attached) is:

$$Av(w/load) = -\left(\frac{RC \parallel RL}{re + R3} \right) \approx -6$$

Step 8) Set values for CC1, CC2, CB1:

- The impedance of a capacitor Zc = 1/j2πfC, make CC1, CC2, & CB1 to look like a 'short' at 10kHz (the input frequency), and match a value found in your ECE 20 kit.