EXPERIMENT 9. J-K Flip-Flop

Equipment and parts required:

1 TTL J-K Flip Flop (7476)
1 Power Supply
1 Digital Voltmeter
1 Function Generator
1 Digital Oscilloscope

1. Find data sheet and specifications

Find I/O pin numbers and specifications of all ICs from data sheet downloaded from the web (ECE labs)

Pin numbers: Vcc, ground, input and outputs of all gates.
Absolute maximum voltages: Vcc and voltages at input pins.
Normal operating voltages: V_{IL}, V_{IH}, V_{OL}, V_{OH}

2. Connect power supply

Adjust the power supply at 5 Volts and set the current limit to maximum. Then connect the power supply to Vcc and Gnd bus. Do not connect the power to the integrated circuit at this time.

3. Calibrate function generator

Adjust the function generator to generate 1 Hz 0-5 Volt clock pulse.

4. Reset Flip-Flop

Find logic inputs J and K to set the flip-flop to Q=0 and Q=1, respectively, and confirm the operation in the experiment.

J	K	Q
		0
		1

5. Measure input and output characteristics of J-K Flip-Flop

Connect the clock from the function generator to the J-K flip-flop, and measure the transition characteristics of the J-K flip flop.

Input J	Input K	Q(t)	Q(t+1)
0	0	0	
		1	
0	1	0	
		1	
1	0	0	
		1	
1	1	0	
		1	

6. Required inputs for desired transitions

Using the results from Step 5, fill out the following table. No extra testing of the chip needs to be performed.

Q(t)	Q(t+1)	J	K
0	0		
0	1		
1	0		
1	1		