

ECE140: Design of Logic Systems I  
Laboratory #12: Intro to Verilog / Xilinx ISE Intro  
*Modified Spring 2012*

During this lab you will learn how to create a new project in Xilinx Project Navigator, how to create a new Verilog code file, how to synthesize it, and how to perform a basic simulation. This lab employs simple Verilog code for a half-adder.

1. Create a new Verilog project:
  - a. Open the **Xilinx ISE Design Suite 13.2** (Project Navigator) software.
  - b. Select File -> New Project.
  - c. Set the project name as **half\_adder** and the location as a new folder in My Documents.
  - d. Select the following values in the Device Properties window:
    - i. Product category: **All**
    - ii. Family: **Spartan 3E**
    - iii. Device: **XC3S250E**
    - iv. Package: **CP132**
    - v. Speed: **-4**
    - vi. Synthesis Tool: **XST (VHDL/Verilog)**
    - vii. Simulator: **ISim (VHDL/Verilog)**
    - viii. Preferred Language: **Verilog**
    - ix. The remainder of the values in the Device Properties parameters are left default. Click Next.
  - e. Skip the rest of the New Project Wizard. Click on Finish.
2. Click on File -> New. Select Text File. Enter the below Verilog code and save the file under the name **half\_adder.v**.

```
module half_adder (A, B, Sum, C_out);  
  
    input A, B;  
    output Sum, C_out;  
  
    xor (Sum, A, B);  
    and (C_out, A, B);  
  
endmodule
```

3. Click on Project -> Add Source. Select the Verilog file you have just created and click OK.
4. Click on Process -> Implement Top Module.
5. After the top module is implemented, under Processes, open up Design Summary/Reports. You will see a tabular summary on the right-hand side of your screen. Obtain a screenshot of the summary.
6. Add a test bench to the project hierarchy.
  - a. Change the view in the left-hand window pane from Design view to Libraries view

- b. Right click in the pane and click on New Source.
  - c. Choose Verilog Test Fixture and name it **half\_adder\_tb**. Click Next.
  - d. Make sure that **half\_adder** is highlighted in the Associate Source window. Click Next and then Finish.
7. The test-bench now opens up in Project Navigator. Scroll to line 45 and 46. Make sure that inputs A and B are initialized to 0 and 0, respectively.
8. Perform a Place and Route Simulation.
  - a. Click on Process -> Implement Top Module. Wait for the implementation to complete.
  - b. In the Design view of the left-hand window panel, change the Design from radio button from Implementation to **Post-Route Simulation**.
  - c. In the hierarchy pane, click on the test bench that was created (half\_adder\_tb).
  - d. In the Processes window pane right below the Design window pane, expand ISim Simulator.
  - e. Double-click **Simulate Post-Place & Route Model**.
9. This simple introductory simulation is performed and ISim opens to view the resultant waveforms which appears in the top right side of the window. Take a screenshot and crop it to only show the waveforms, like you saw in the presentation.
10. Close ISim. Do not save the results. Open up the half\_adder\_tb file (if it is not already open) and scroll to lines 45 and 46. Edit line 46 such that input B initializes to 1. Save the test-bench file and repeat steps 8 and 9.
11. Repeat step 10, this time editing lines 45 and 46 such that A is initialized to 1 and B is initialized to 0.
12. Repeat step 10, this time editing lines 45 and 46 such that A is initialized to 1 and B is initialized to 1.
13. **Explain why the waveforms are correct; provide a truth-table that summarizes what is happening in the waveforms.**