GAL JEDEC File Generation

1. Open ispLEVER software:
   Start > All Programs > Lattice Semiconductor ispLEVER Classic 1.4 > **Classic Project Navigator**

2. Create a new project using the Project Wizard:
   File > New Project

3. Set up the project with these settings:

   a. Project Name: Give your project a unique name.

   b. Location: Click on  to the right of Location text box. Navigate to where you want to save the files (either the desktop, documents, or a flash drive) and create a folder (using the **Make New Folder** button) for your project files. Select this folder and then click on **Ok**.

   c. Design Entry Type: Verilog HDL

   d. Synthesis Tools: Synplify

   Click on **Next** to continue.

4. Select the device according to the device you're using. Make sure the **Part Name** is set to the part number on your IC.
   For ECE 2140 part kits, set device according to the following:

Family	GAL Device
Device	GAL16V8D
Part Name	GAL16V8D-15QP

Click on Next to continue.

5. Do not enter anything in the **Add Source** page – click on **Next** to continue to the **Summary** page. Verify the settings on this page, and click on **Finish** if all the settings are correct.

6. Create a new Verilog source file:
   Source > New
   Select **Verilog Module** and click **Ok**.

7. Enter the settings:

Module Name	half_adder
File Name	half_adder.v

Click on **Ok** to create the Verilog file.

8. A text editor will open with a simple Verilog module definition. **Put your Verilog code in this window.**

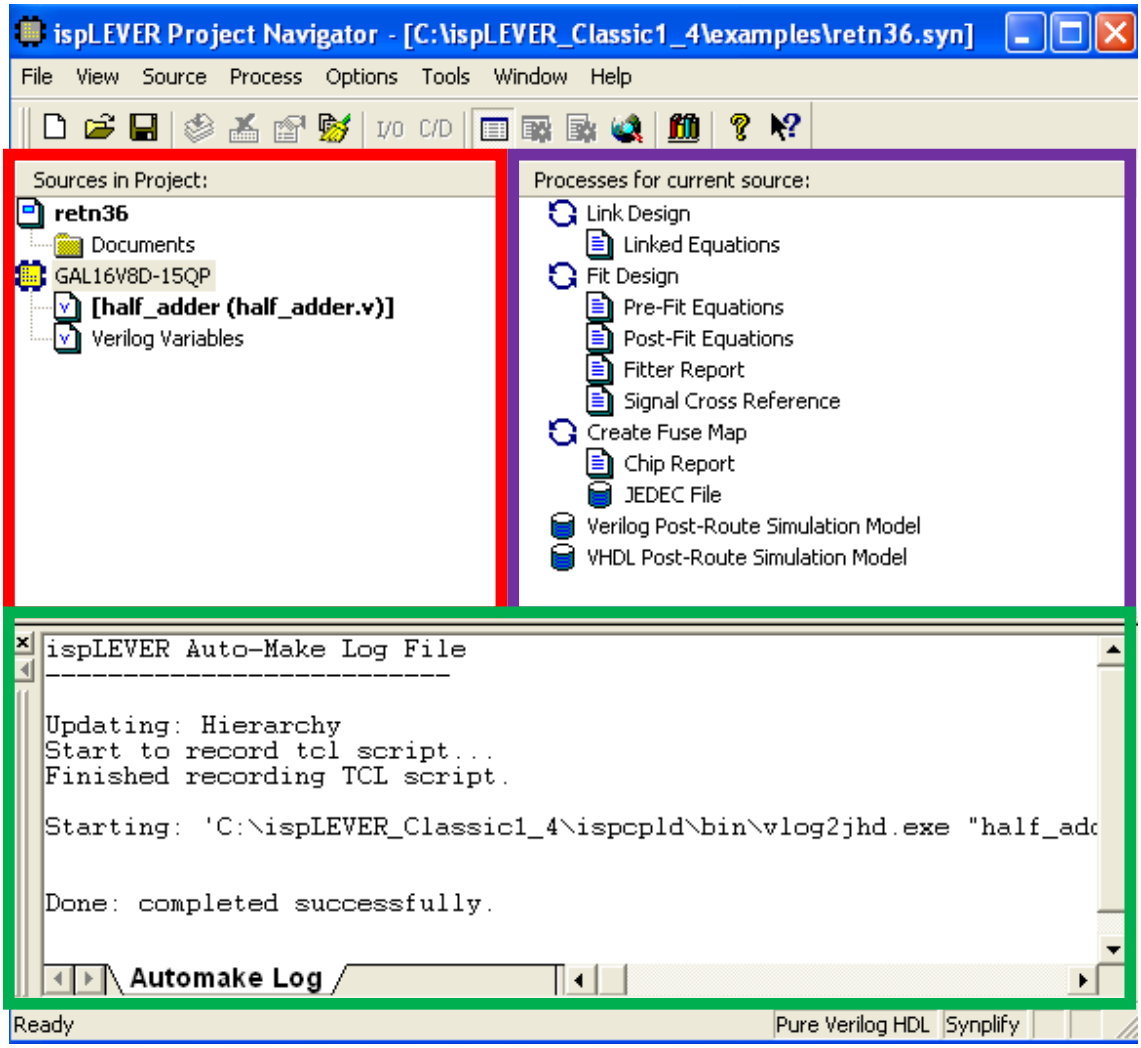
9. When you are finished editing the Verilog module, save and close the Verilog file:
   File > Save then File > Exit

10. You should now be back in the main window of ispLEVER Project Navigator. ispLEVER has 3 main components:

    a. Sources (outlined in red)

    b. Processes for select source (outlined in purpose)

    c. Log viewer (outlined in green)



11. Generate programming files:

    a. In ***Sources*** component, click once on **GAL16V8D-15QP** to select it.

    b. In the ***Processes*** component, double-click on **JEDEC File**. The application will synthesize your Verilog code and create a programming file for the GAL.

c. When it is complete, **Done: completed successfully** will be displayed at the bottom of the ***Log viewer***. If you have any errors, go back and fix the problem before proceeding.

12. Find the pin mapping:

    a. In the **Processes** component, double-click on **Chip Report**

    b. The pin mapping will show up in the log viewer.

13. The JEDEC programming file will be located in your projects directory (was set in the Project Wizard). Look for the file named ***your_project_name*.jed**