

**The George Washington University
Department of Electrical and Computer Engineering**

ECE 2140: Design of Logic Systems I

Final Projects Revised Spring 2012

Presentation

The goal of your final project is to reuse the knowledge you have acquired during the semester to realize a complete project. You will have to go through (and document) all the phases of the conception (specification, architecture design, detailed design, implementation and tests).

Projects are to be realized strictly individually. Remember, GW's Academic Integrity Code still applies.

If you choose a project using Digilent Basys Xilinx boards, keep in mind that you won't be able to borrow a board of the school to use outside of lab. You will have to test your code using the Xilinx ISE simulation tool. (The design will still be tested on the board during the presentation).

The due date for the report is **May 1st** (on Blackboard). But you will have to make a small presentation of 5 minutes, include a demonstration of the working design during the last laboratory session.

Project Report Format

- 1 Introduction
- 2 Specifications
- 3 Design
 - 3.1 Overview
 - 3.2 Schematics
- 4 Implementation
 - 4.1 Overview/Procedure
 - 4.2 Verilog source code (must be in TEXT form, not an image of the code)
 - 4.3 Simulation (if necessary)
 - 4.4 Results
- 5 Conclusion

Choose 1 of the following projects:

1 Chronograph

On the Digilent Basys (or Basys2) FPGA board, design a chronograph. It should have the following functionality:

- ⤴ Seconds display on the LEDs
- ⤴ Start/Stop switch
- ⤴ Reset/hold switch – if pressed while time is running, will freeze time displayed on LEDs (while still counting time in the background). After switch is moved back, the LEDs will display current time. If pressed while time is NOT running, will reset timer back to 0.

2 Counter

Build a one-digit counter using discrete integrated circuit (IC) components. Result must be displayed using 7-segment displays.

3 2-bit ALU

Design a two-bit ALU in Verilog. Implement it on the Digilent Basys (or Basys2) FPGA board. Build a test circuit for it.

Operation	Operation code	Result
Left shift	000	$C = A_00, Carry = A_1$
Right shift	001	$C = 0A_1, Carry = 0$
Addition	010	$C = A + B$
Substraction	011	$C = A - B$
XOR	100	$C = A \text{ xor } B$
Or	101	$C = A \text{ or } B$
And	110	$C = A \text{ and } B$
Set	111	$C = 11, Carry = 1$

