ECE 2140
Experiment 10
Half-Adder on Gate Array Logic

Equipment and Parts Required

- 1 GAL (16V8 or equivalent)
- 1 DC Power Supply
- 1 Digital Voltmeter

1. Write a Verilog program for a half-adder

Print the source code from the ispLEVER editor window, and attach it to the report.

```
module half_adder(x,y, sum, carry );

input x;
input y;
output sum;
output carry;


assign sum = x ^ y;
assign carry = x & y;


endmodule
```

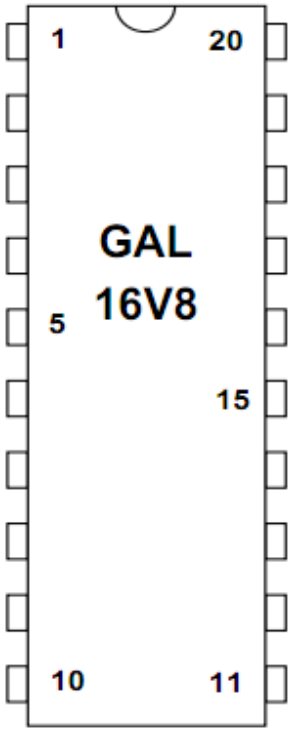
2. Compile the Verilog code using ispLEVER

Follow the instructions posted on the course website to compile Verilog.
(http://www.seas.gwu.edu/~ece140/2011-spring/files/GAL_ispLEVER.pdf)

Describe the detailed steps to compile your source code in ispLEVER.

3. Label the pins used for your 16V8 GAL after you compile & synthesize

Make sure to include this in your lab report.



4. Program the GAL chip using the JEDEC file created in step 2

Refer to the instructions on the course website
(http://www.seas.gwu.edu/~ecelabs/appnotes/PDF/dataio.pdf)

Describe the procedure to program the GAL chip in your lab report.

5. Experiment with your programmed GAL chip, and fill out the following truth table

X (Volts)	Y (Volts)	Sum (Volts)	Carry (Volts)
0	0		
0	5		
5	0		
5	5		

6. What are the pros and cons of using programmable logic devices such as the GAL chip?