YK Inc. is awarded a contract to improve and update the Metro computer system. One part of the Metro system that needs improvement is the fare card controller. The digital design group of YK Inc. is given a task to design, fabricate, and test a low cost, monolithic IC-based fare card controller employing CMOS technology.

The Metro system has 16 stations. Each metro station needs controller modules to perform the following tasks:
0. Check-in (At entry – “00”)
1. Check-out (At exit – “01”)
2. Fare Adder before entry (if necessary – “10”)
3. Fare Adder before exit (if necessary – “11”)

Each station has a 4-bit station identification number, \( N \), where, \( 0 \leq N \leq 15 \). The cost of a one-way trip to any station is calculated as follows:

Non-rush hour cost (in dollars) = \( 0.50 + |N_{\text{in}} - N_{\text{out}}| \times 0.25 \)
Rush hour cost (in dollars) = \( 1.00 + |N_{\text{in}} - N_{\text{out}}| \times 0.25 \)

A fare card can have a maximum value of twenty dollars. The information on the fare card is stored in 16 bits, according to the following diagram:

| Header (4-bits: “1010”) | Balance (7-bits: 25 cent increments) | Time Stamp (1-bit) | \( N_{\text{in}} \) (4-bits) |
The purpose of the "1010" header is to indicate that up to 12 more bits of information are to be read by the controller. The balance indicates the remaining balance on the fare card in 25 cent increments, e.g., "0000100" corresponds to one dollar. The one-bit time stamp indicates non-rush hour ("0") and rush-hour ("1"), respectively. The last 4-bits indicate the entry station identification number, $N_e$. Note that, prior to entry, the time stamp and station identification fields must have been set to zero.

When a passenger enters the station, the system will read the information from the fare card (only header and balance) and determine if the fare card has sufficient funds for a minimum one-way trip in accordance with the time of the day. If the amount is insufficient, the card controller will generate an insufficient fund signal (Gate Open = 0). If the amount on the fare card is sufficient, the system will first reset/erase the fare card (by writing 16 zeroes) and then write the full 16-bit information, which now includes the time stamp and station ID information. The system will return the card to the passenger, and open the gate (Gate Open=1).

When a passenger is exiting the station, the system will read the 16-bit information from the fare card. The system will then calculate the fare based on entry station ID, exit station ID and time stamp based on the above formulas. If the amount is insufficient, the card controller will generate an insufficient fund signal (Gate Open = 0). If the amount on the fare card is sufficient, the system will first reset/erase the fare card (by writing 16 zeroes) and then write the header, and update the balance. It will then generate a gate open signal.

When a passenger needs to add new funds to the card, the fare adder function will update the balance based on added funds. It will do so by first resetting the fare card to zero and then writing the new 16-bit field (which includes the updated balance).

The whole operation of reading the input from fare card, processing the data, updating the fare card information and opening the gate must be less than 1 second. Each bit duration is 10 milliseconds. The designer is responsible for designing a separate circuit that generates an appropriate clock.

The designer is required to design, simulate, layout, and verify his/her design using the Tanner Tools CAD program. It is the designer’s responsibility to make sure that the correct pulses are generated and the timing requirements are met. The circuit must be implemented in 0.8 micron HP CMOS n-well technology, except for the clock circuit, which can be presented in schematic (S-Edit) form. A 5 VDC power-supply is available. In the documentation, the designer must clearly demonstrate the correct operation of the circuit for at least five different test cases and be able to demonstrate one-random case upon request.

Complete engineering documentation of designer’s work is required. The documentation should be concise and complete. The due date for the presentation, demonstration and documentation is Wednesday, December 11, 2002.